Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

THIRD SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION
NOV 2017
SUBJECT: LOGIC DESIGN (ECE - 2105)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Simplify the following Boolean expression using:
(i) Quine Mc-Cluskey method
(ii) VEM with 'd' as the map entered variable
(iii) Whether results obtained from (i) and (ii) are same or not?
f(a, b, c, d) = ∑m (0, 2, 3, 4, 8, 10, 12, 13, 14)

1B. Find the minimal product(POS) and minimal sum (SOP) expression for the function given below:
$$f(A,B,C,D) = \overline{A}\,\overline{B}D + BCD + A\overline{B}D + B\overline{C}\,\overline{D}$$

1C. Define the following:
(i) Noise margin (ii) Propagation delay

(5+3+2)

2A. Consider a 2-bit magnitude comparator as shown in Figure Q2A, with two outputs "Equal (E)" and "Not-equal (NE)". Note the inputs to the comparator are – input X = A1B1 and input Y = A0B0.
(i) Implement the output E using an 8:1 multiplexer.
(ii) Implement the output NE using 1-bit magnitude comparator modules.

2B. Implement the following function using active low 2:4 and 3:8 decoders. F(w,x,y,z)=∑m(0,1,5,9,12,14,21,25)

2C. What is a self-complementing code? Verify whether 2421 is self-complementing or not.

(5+3+2)

3A. Design a 4-bit multiplier which multiplies $a_3a_2a_1a_0$ and $b_3b_2b_1b_0$ using half adders, full adders and AND gates only.

3B. Design a 3 bit shift-register which shifts data from left to right when control signal S='0' and shifts data from right to left when S='1' using positive edge triggered D flip-flop.

3C. Realize a negative edge triggered T flip-flop using a negative edge triggered D flip-flop.

(5+3+2)

4A. Design a synchronous sequential circuit which has two serial binary inputs X and Y and one serial out Z such that Z is '1' whenever input sequence is "01", "10", and "11". Use T flip-flops for implementation.

4B. Draw the circuit diagram of Master-Slave JK flip-flop using basic gates and write the truth table. Explain how race around condition is avoided in it.

4C. Write ASM chart for a 3 bit synchronous down counter.

(5+3+2)

5A. Design a fundamental mode asynchronous sequential circuit using D latch which satisfies following conditions-

i) It has two inputs T and G and one output Q.

ii) When G='0', Q remains same irrespective of changes on T.

iii) When G='1', Q toggles its state.

5B. Realize f1=∑m (0, 1, 4) and f2=∑m (2, 3, 4, 7) using 3×4×2 PLA.

5C. Show how the frequency of train of pulses can be divided by 4 using flip-flops.

(5+3+2)

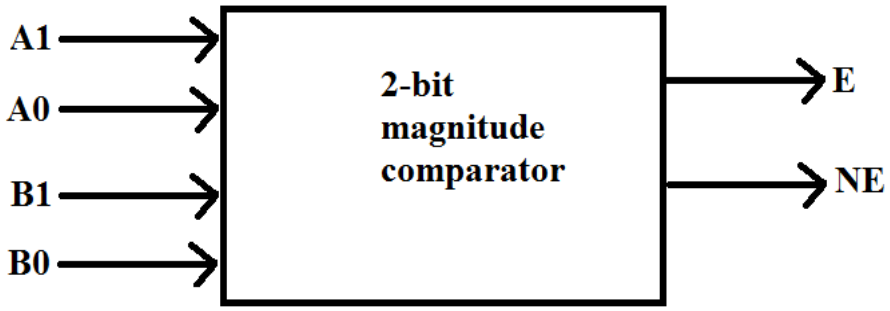

Figure Q2A