Reg. No.

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

III SEMESTER B.TECH. (INFORMATION TECHNOLOGY)

MAKEUP EXAMINATIONS, DEC 2017/JAN 2018

SUBJECT: DIGITAL SYSTEMS [ICT 2102]

REVISED CREDIT SYSTEM
(22 /12 /2017)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer ALL the questions.
- Missing data, if any, may be suitably assumed.

1A. Simplify the given function 'F' using tabulation method. Implement the simplified expression using basic logic gates. 5

$$F(A,B,C,D,E) = \sum m(0,2,4,6,9,10,12,18,21,25,27) + \sum d(3,8,20,22,30)$$

1B. Using basic gates, design a 1 – bit magnitude comparator with cascading inputs. Use this design and give the block diagram representation of 2 – bit magnitude comparator. 3

1C. Design a T flip flop from SR flip flop. 2

2A. Design a synchronous sequential circuit using Moore model, with one input A and one output Y. The output Y is to be HIGH whenever the sequence "100111" is detected. Otherwise the output is LOW. Overlapping of the sequence is allowed. Implement using T- flip flops and external gates. 5

2B. Design a sequential logic circuit to generate a binary sequence 10110010 using Johnson counter. 3

2C. Explain 4:2 priority encoder with necessary truth table, circuit diagrams. 2

3A. Design a combinational circuit to evaluate the arithmetic expression $D = X^2 - Y^2$ using 7483 IC and external gates, where X and Y are 2- bit binary numbers. 5

3B. Implement a full subtractor using a suitable PLA. 3

3C. Using 7490 ICs only, design a logic circuit which divides the frequency of the input square wave by a factor of '100' and produces an output waveform with 50 percent duty cycle. 2

4A. Design a code converter to convert a decimal digit represented in 2421 to decimal digit represented in 8 4 2 1 code, using NOR gates only. 5

4B. What is a race around condition? How is it overcome using Master Slave configuration? Give necessary circuit diagrams and waveforms. 5

4C. Design 5: 32 decoder using 3 to 8 decoders only. 2

5A. Design a self-starting synchronous counter using T – flip flops and external gates to count the sequence 1 → 2 → 4 → 9 → 12 → 5 →1. 5

5B. Design a 3-bit carry look ahead adder. 3

5C. Realize the boolean function $F(A,B,C,D) = \sum m(0,1,3,5,6,8,10,11,15)$ using 74153 ICs only 2