Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

III SEMESTER B.TECH. (INFORMATION TECHNOLOGY)

END SEMESTER EXAMINATIONS, NOVEMBER 2017

SUBJECT: DIGITAL SYSTEMS [ICT 2102]

REVISED CREDIT SYSTEM
(18 / 11 /2017)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data, if any, may be suitably assumed.

1A. Design a synchronous sequential circuit using Mealy model, with one input X and one output Y. The output Y is to be HIGH whenever the sequence "0100101" is detected. Otherwise the output is LOW. Overlapping of the sequence is allowed. Implement using D- flip flops and external gates. **5**

1B. Design a 2-bit subtractor using 74153 ICs and external gates. **3**

1C. Design 5:32 decoder using 74138 ICs and one external gate. **2**

2A. Design a code converter to convert a decimal digit represented in Excess-3 to decimal digit represented in 8 4 -2 -1 code, using NAND gates only. **5**

2B. Using a suitable PROM, implement a logic function to perform the square of a 3-bit binary number. **3**

2C. Design a 3-bit bi-directional shift register using D flip flops, 2:1 MUXs and external gates. **2**

3A. Design a 3-bit synchronous gray code UP/DOWN counter using JK flip flops and external gates. **5**

3B. Design a single digit decimal adder using 7483 ICs and external NAND gates. **3**

3C. Design 8 – bit binary UP counter to count from N_1 to N_2 using 74193 ICs, 7485 ICs and external gates. Assume $N_1 < N_2$. **2**

4A. Simplify the given function 'F' using tabulation method. Implement the simplified expression using basic logic gates. 5

$$F(A,B,C,D,E) = \sum m(3,5,6,9,11,12,15,21,25,27) + \sum d(2,8,20,22,30)$$

4B. Design a MOD 9 asynchronous down counter using T flip flops. Using the same, generate the sequence 110010010. Use external gates if required. 3

4C. Why is Carry Look Ahead adder faster than Carry Propagation adder? 2

5A. Design 4 – bit × 4 – bit binary multiplier using 7483 ICs and minimum number of external NAND gates. 5

5B. Design a 3-bit magnitude comparator using logic gates. 3

5C. Design a D flip flop using JK flip flop. 2