Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

THIRD SEMESTER B.TECH. (INSTRUMENTATION AND CONTROL ENGG.)

END SEMESTER EXAMINATIONS, NOV - 2017

SUBJECT: DIGITAL ELECTRONIC CIRCUTS [ICE 2103]

Duration: 3 Hour Max. Marks:50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A Match the following: 2

a.	XS-3 code	i	XOR gate
b.	Anti-coincidence Detector	ii	Gray Code
c.	Equality detector	iii	Biquinary
d.	Uni-distance Code	iv	Self-complementary 8421 code
		vi	XNOR gate

1B Realize the circuit shown in FIG Q.1B, using only 2 input NAND gates. 3

1C Minimize the following expression using Quine-McCluskey method. 5
$f(A,B,C,D)=\Sigma m(1,2,3,5,9,12,14,15)+ \Sigma d(4,8,11)$

2A In a certain chemical-processing plant, a liquid chemical is used in a manufacturing process. The chemical is stored in three different tanks. A level sensor in each tank produces a HIGH voltage when the level of chemical in the tank drops below a specified point. Design a circuit that monitors the chemical level in each tank and indicates when the level in any two of the tanks drops below the specified point. 2

2B Design and implement a Full Subtractor using Demultiplexer. 4

2C Explain four bit addition using carry look ahead logic with suitable diagram. 4

3A A given flip-flop is found to produce a toggling output state when both of its inputs are given active HIGH. Identify the flip-flop. Also, explain the cause of this output condition with proper diagrams. 2

3B Convert SR flip-flop into T flip-flop and draw the logic diagram. 3

3C Design and implement the synchronous gray-code up counter using JK flip-flops. 5

4A Construct the truth table for the circuit shown in FIG Q.4A. 3

4B Explain the working of 4-bit parallel in serial out shift register using load and shift capability with help of neat diagram. 4

4C	Bring out the difference between i) Moore and Mealy Model ii) Static and Dynamic hazards.	3
5A	State various applications of Shift register.	2
5B	Design a BCD to Excess-3 code converter and implement using PAL.	4
5C	Analyze the sequential circuit shown in FIG Q.5C and draw the state diagram.	4

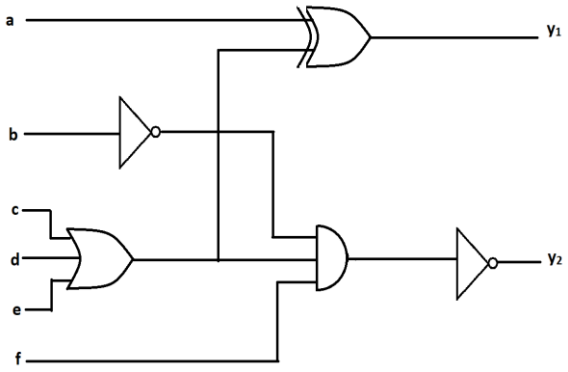

FIG Q.1B

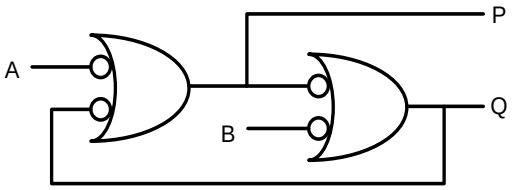

FIG Q.4A

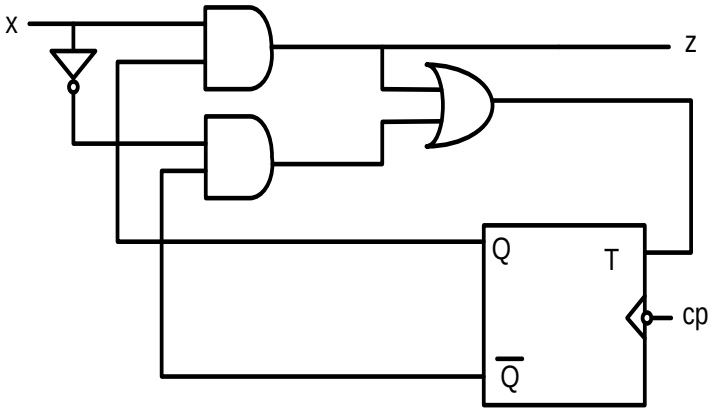

FIG Q.5C