Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

III SEMESTER B.TECH. (MECHATRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, DEC 2017

SUBJECT: DIGITAL INTEGRATED CIRCUIT APPLICATION [MTE 2105]

REVISED CREDIT SYSTEM
MAKE UP EXAM
(25/11/2017)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Data not provided may be suitably assumed

1A. The message 1110110 coded using 7-bit Hamming code is transmitted through a noisy channel. Decode the message assuming that at most a single error occurred in each code word **2**

1B. Design a Mealy type sequence detector to detect the sequence 10111. Overlapping of sequences is permitted and use D flip flops. **5**

1C. Design a 4 bit ring counter using D flip flops. Draw the timing diagram and note the output sequence **3**

2A. Design one input one output serial 2's complementer. The circuit accepts a string of bits from the input and generates the 2's complement at the output. The circuit can be reset asynchronously to start and end operation. **4**

2B. An industrial robot that places components on a PCB has 3 fail safe sensors and an emergency shutdown switch. The robot should keep functioning unless any any of the following conditions arise: **4**
If the emergency switch is pressed the system shut down.
If the sensor 1 & sensor 2 are activated at the same time the system shutdown.
If the sensor 2 & sensor 3 are activated at the same time the system shutdown.
If all three sensors are activated at the same time then the system shutdown.
Derive the truth table for this system
Design using K-Map, a minimum AND-OR gate network for this system
Design a digital circuit which will implement the minimal AND-OR gate network found in (b) using both (i)NAND gates only and (ii) NOR gates only
If the time delay experienced by a NAND gate is 10ns and the time delay experienced in a NOR gate is 8ns. Which implementation of (c) is faster? By how long?

2C. Design a 1-bit comparator using decoder **2**

3A.	What is a priority encoder? How is it different from encoder? Design a 3-bit priority encoder and explain.	**4**
3B.	Realize full adder using CMOS semiconductor device.	**3**
3C.	Draw the state diagram for Mealy and Moore Model for sequence detector circuit for 1101 sequence with overlapping allowed	**3**
4A.	Design a serial binary adder as a Moore Machine using D flip flop.	**5**
4B.	Explain with the waveform the working of Johnson ring counter.	**3**
4C.	Implement 4-bit combinational incrementer using four half adders. (A circuit that adds one to a four-bit binary number).	**2**
5A.	A PN flip-flop has four operations: clear to 0, no change, complement, and set to 1, when inputs P and N are 00, 01, 10, and 11. Respectively. (a) Tabulate characteristic table (b) Derive characteristic equation (c) Tabulate excitation table (d) Show how PN flip-flop can be converted in to D flip flop	**5**
5B.	Explain classification of codes in number system	**2**
5C.	Convert SR Flip-flop to JK Flip-flop	**3**