Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

III SEMESTER B.TECH. (MECHATRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, NOV 2017

SUBJECT: DIGITAL INTEGRATED CIRCUIT APPLICATION [MTE 2105]

REVISED CREDIT SYSTEM
(25/11/2017)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Data not provided may be suitably assumed

1A. Design MOD-18 Asynchronous negative edge triggered up counter **3**

1B. Implement given four Boolean expressions in a circuit using three half adders **3**

$D=A\oplus B\oplus C$; $E=\overline{A}BC + A\overline{B}C$; $F = AB\overline{C} + (\overline{A}+\overline{B})C$; $G=ABC$

1C. Design a circuit for generating the following sequence using D flip flop shown in Fig : Q1C. **4**

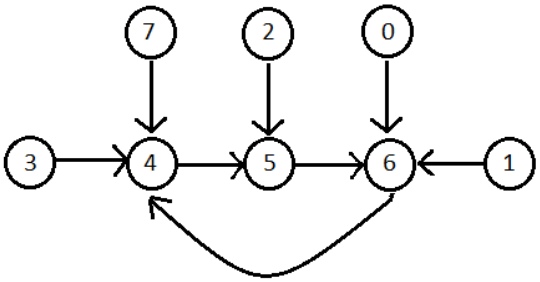

Fig : Q1C

2A. The message below coded in the 7-bit Hamming code is transmitted through a noisy channel. Decode the message assuming that at most a single error occurred in each code word- 1001001 , 0111001 , 1110110 , 0011011 **3**
Also name other error detecting codes.

2B. An automobile alarm circuit is used to detect certain undesirable conditions. Three switches are used to indicate the status, which are the door by the driver's seat , the ignition, and the headlights respectively. Design a logic circuit and write down the minimal expression for output with these switches as inputs so that alarm will be activated whenever either of the following conditions exists: **3**

i)The headlights are ON while the ignition is OFF.

ii)The door is open while the ignition is ON.

Also implement the circuit using De-multiplexer

2C. Design the circuit using logic gated that gives output as 1 when a 4 bit BCD code translated to a number that lightens the upper right segment of a seven segment display. **4**

3A. Design a serial adder circuit using Mealy Model representation with D flip flop. **5**

3B. Assuming that all Flip-Flops shown in Fig :Q3B are in reset condition initially, mention the count sequence that is observed at terminal $Q_{(A)}$ in the circuit shown for next 6 clock pulses. **2**

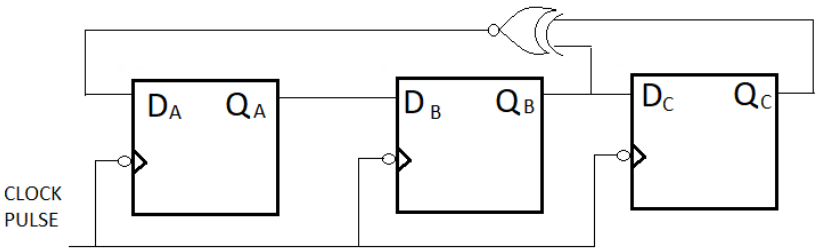

Fig : Q3B

3C. Perform subtraction of 324.7-108.9 (given in decimal number system) using- **3**
i)Excess-3 subtraction

ii) 10's complement rule.

4A. A serial parity generator is a sequential circuit that receives an n-bit message followed by a '0' or '1'.Draw state diagram for a 3-bit serial odd parity generator which replaces the 'n+1'th bit with odd parity. **3**

4B. Draw the output waveform for the diagram shown in Fig : Q4B for negative edge triggered JK flip flop with initial output as zero. **3**

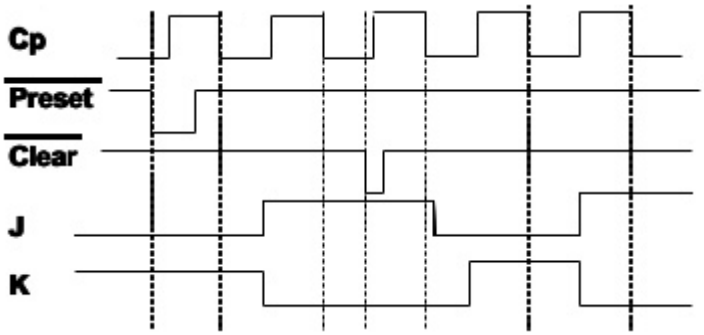

Fig : Q4B

4C. Draw the state diagram for NAND and NOR latch using transition table and flow table. **4**

5A. Design 4 bit BCD adder using 74LS283 IC and additional logic gates. **3**

5B. Realize full subtractor using CMOS semiconductor device **4**

5C. For the given expression $f(A,B,C,D)=\sum m(0,1,2,4,6,9)+\sum d(3,7,10,11,14,15)$. Find the minimal expression and essential prime implicants. **3**