Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

III SEMESTER B.TECH. (MECHATRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, DEC/JAN 2017

SUBJECT: Linear Integrated Circuits & Applications [MTE 2104]

REVISED CREDIT SYSTEM

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitable assumed.

1A. Derive the expressions for input resistance, output resistance and voltage gain of inverting amplifier with the help of equivalent circuit of op-amp. **(4M)**

1B. Find gain in the circuit shown below **Fig.Q1 (B)**, if all resistances are equal. **(3M)**

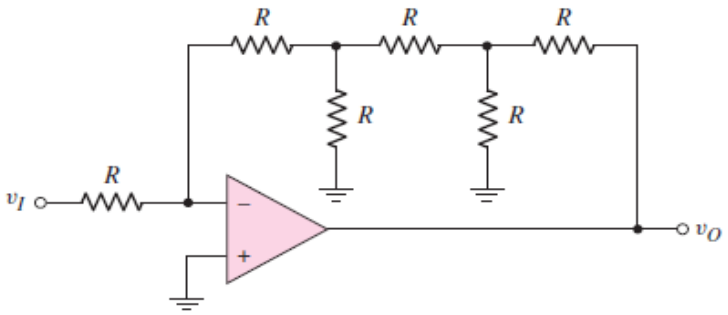

Fig.Q1 (B)

1C. Design a wide band reject filter having f_H = 400 HZ and f_L = 2KHZ with a pass band gain of 2 **(3M)**

2A. Derive time period expression for triangular wave generator using OP-AMP. Calculate the component values required for triangular wave generator to generate output frequency = 5kHz and Vo (pp)=10.5 V. **(4M)**

2B. Design a circuit that provides modulus of the input (sine wave) at the output. **(3M)**

2C. With the help of circuits and necessary equations, explain how multiplication can be performed using IC 741. **(3M)**

3A. For the circuit shown in **Fig.Q3 (A)**, calculate the values of R1 and R2 if saturation voltages are +12 V and -12V. Assume hysteresis width = 6V **(3M)**

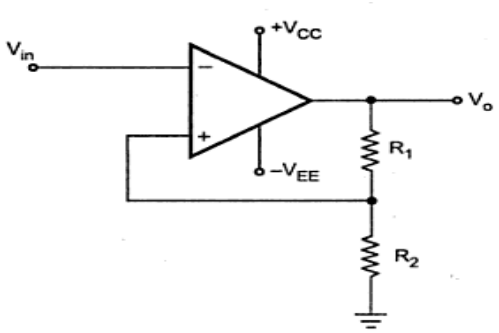

Fig.Q3 (A)

3B. Design an op-amp circuit to generate a pulse waveform of frequency 2 kHz **(3M)**

3C. Derive transfer function of All-pass filter and also obtain magnitude and phase angle from transfer function. **(4M)**

4A. Design a timer using 555 IC to generate frequency of 1kHz at 50% duty cycle. Connect one RED LED & one GREEN LED so that for 0.5ms the RED LED is ON and GREEN is OFF and for the next 0.5ms the GREEN LED is ON and RED if OFF. LEDs power supply rating is 5V and 50mA. **(4M)**

4B. Design frequency multiplier circuit using PLL IC 565 to multiply input frequency by 16, Centre frequency is 70KHZ. Find lock and capture frequency at output and state related tracking range and capture range limits for input. **(4M)**

4C. A PLL has free running frequency of 700 kHz and bandwidth of the LPF is 100KHz.Will the loop acquire lock for an input signal of 400 kHz? Justify your Answer. **(2M)**

5A. Suggest an ADC that takes equal conversion time for any sample. Explain its operation with the help of circuit diagram. **(3M)**

5B. For a 566 VCO shown in **Fig.Q5 (B)**, +V = 10 V, R2 = 1.2 KΩ and R1=R3= 10KΩ with C1=0.001μF. Calculate the frequency of output; calculate the variation in fo if V_C is varied between 7.7 and 9.5 V. Also draw the square wave output if modulating input is sine wave. **(3M)**

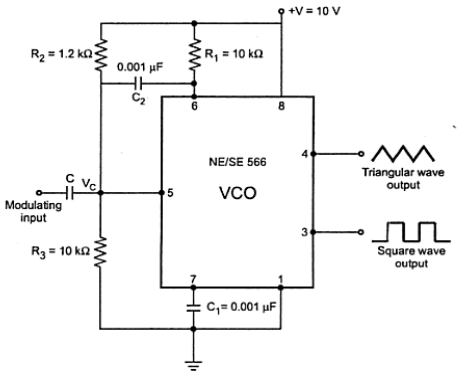

Fig.Q5 (B)

5C. Draw the functional diagram of LM 317 with protective circuit and derive output voltage equation. Find the range in which output voltage can be varied with the help of LM 317 regulator using R1 = 820Ω and R2 = 10KΩ potentiometer.[For LM 317 I_{ADJ} = 100μA] **(4M)**