MANIPAL
ACADEMY of HIGHER EDUCATION
(Deemed to be University under Section 3 of the UGC Act, 1956)

Reg. No.										

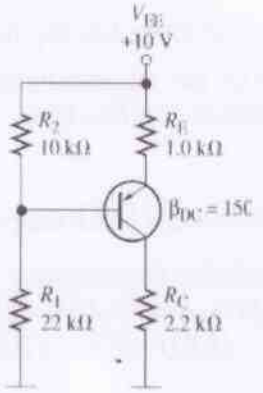
DEPARTMENT OF SCIENCES, I SEMESTER M.Sc (PHYSICS)
END SEMESTER EXAMINATIONS 2017
MAKE-UP
Subject : FUNDAMENTALS OF ELECTRONICS (PHY 4107)
(REVISED CREDIT SYSTEM-2017)

Time: 3 Hours Date:23-12-2017 MAX.MARKS: 50

Note: Answer all **FIVE FULL** questions

1(A) Define quality factor. Obtain an expression for quality factor for a series RLC circuit and arrive at a relationship between bandwidth and quality factor. (4)

1(B) Find I_C and V_{EC} in the following circuit.



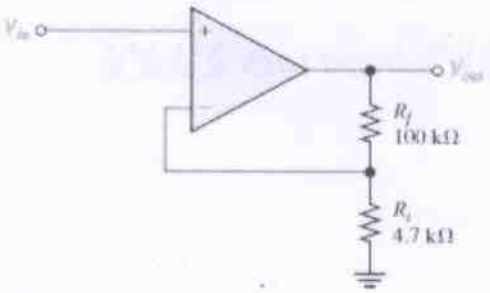
(4)

1(c) Draw an equivalent circuit of an UJT and define its intrinsic stand off ratio. (2)

2(a) Draw the basic differential amplifier circuit and its ac equivalent circuit.Derive an expression for the single ended voltage gain. (4)

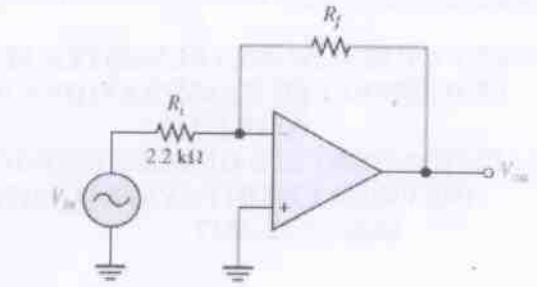
2(b)

(i) Determine the closed-loop voltage gain of the amplifier given below:



(2)

(ii) Given the op-amp configuration in Figure below, determine the value of R_f required to produce a closed-loop voltage gain of -100.



(2)

2(c) Draw the circuit diagram of an op-amp integrator. (2)

3(a) Discuss the operation of Schmitt trigger. (3)

3(b) Explain how timer 555 can be used as monostable multivibrator. (4)

3(c) Draw the circuit diagram of first order low pass filter and discuss its operation. (3)

4(a) Sketch the logic system for a clocked J-K flip flop.Give its truth table and verify it. (4)

4(b) Showing the logic diagram of two bit simultaneous(flash) A/D converter. Explain its working and give logic equations for two bits. (4)

4(c) Define a multiplexer and draw logic block diagram of a 4-to-1 line multiplexer. (2)

5(a) Use a Karnaugh map to minimize the following SOP expressions:

(i) $AB\bar{C}+A\bar{B}C+\bar{A}BC+\bar{A}B\bar{C}+A\bar{B}\bar{C}+ABC$

(ii) $\bar{A}\bar{B}\bar{C}\bar{D}+A\bar{B}CD+A\bar{B}\bar{C}D+\bar{A}CD+A\bar{B}\bar{C}\bar{D}$ (4)

5(b) Give the truth tables of two input NOR ,NAND,EXCLUSIVE-OR and EXCLUSIVE - NOR gates. (4)

5(c) Find the output voltage from a 5 bit ladder that has a digital input of 11010.Assume that 0=oV and 1=10V. (2)

Good Luck