MANIPAL UNIVERSITY

Reg. No.										

Deemed- to -be -University under Section 3 of the UGC Act, 1956

DEPARTMENT OF SCIENCES, I SEMESTER M.Sc (PHYSICS))
END SEMESTER EXAMINATIONS, Nov/Dec 2017

Subject : FUNDAMENTALS OF ELECTRONICS(PHY 4107)

(REVISED CREDIT SYSTEM-2017)

Time: 3 Hours Date:23.11.2017 MAX.MARKS: 50

Note: Answer all **FIVE FULL** questions

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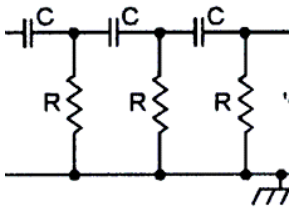
1. (a) Show that the following feedback circuit produces a phase shift of exactly 180^o when the frequency of the signal is given by $f = \frac{1}{2\pi\sqrt{6}\,RC}$

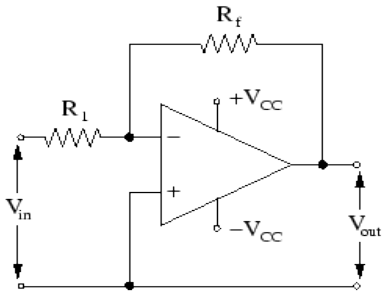


(b) Discuss the frequency response of BJT amplifier in CE configuration .Obtain an expression for lower cut off frequency considering only the effect of coupling capacitor Cs.

(c) Transform the following function of time into the phasor form.

$3\cos 600t - 5\sin(600t+110^o)$ **(4+4+2)**

2. (a) Using the ac equivalent circuit of an op-amp obtain an expression for the voltage gain for the following circuit.



(b)Draw the schematic diagram for the first order active high pass filter and obtain an expression for it's low cut off frequency.

(c) Explain how SCR can be used to control the conduction angle. **(4+4+2)**

3. (a) Draw the circuit diagram of astable multivibrator using Timmer 555 and explain it's action. Arrive at an expression for it's frequency.

(b) Using a neat circuit diagram explain how op amp can be used as an integrater.

(c) Draw a circuit diagram of op-amp series regulator. **(4+4+2)**

4. (a)Giive truth tables for (i) S-R (ii) J-K (iii) D and (iv)T flip flops.

b) Draw the state diagram of a three bit gray counter .Showing the transition table of J-K flip flop obtain Karnaugh map for J and K terminals of the flip flop corresponding to least significant bit .

(c) Show how multiplexer can be used as logic function generator. **(4+4+2)**

5. (a) Draw a schematic diagram of a four bit D/A converter.If 0=0V and 1=10V ,calculate the output voltage produced by most and least significant bits.

(b) Use a Karnaugh map to minimize the following standard SOP expressions:

(i) $A\,\bar{B}C + \bar{A}BC + \bar{A}\bar{B}C + \bar{A}\bar{B}\bar{C} + A\bar{B}\bar{C}$ *(ii)* $\bar{B}\bar{C}\bar{D} + \bar{A}B\bar{C}\bar{D} + AB\bar{C}\bar{D} + \bar{A}\bar{B}CD + A\bar{B}CD$

(c) Draw the symbol and truth table of an exclusive OR gate. Obtain its Boolean expression.

(4+4+2)