Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

FIRST SEMESTER M.TECH DEGREE END SEMESTER EXAMINATION
NOV/DEC 2017
SUBJECT: PROCESSOR ARCHITECTURE & APPLICATIONS (ECE - 5103)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Describe architectural overview, on chip memory of TMS320C67x DSP Processor.

1B. Discuss architecture of memory vector processor.

1C. Explain DMA based I/O strategy with algorithm / program used for implementation.

(4+4+2)

2A. Write a table showing control values for the forwarding multiplexers from hardware forwarding unit and algorithm / pseudo code for EX and MEM hazards. Sketch forwarding unit with inputs and outputs.

2B. With a diagram, show complete single cycle data path implementation scheme for R – type, load store and branch equal instructions.

2C. Interface 4K byte ROM using address decoder and other logic circuits. Address range is 00006000H to 00006FFFH.

(4+4+2)

3A. With necessary sketches, explain mechanism to map main memory to cache using direct mapping. Discuss its disadvantage. How it can be improved by set associative mapping? Explain with examples.

3B. What are the taxonomy of parallel processor architectures? Explain. Also discuss processor interconnect strategy for different memory architectures.

3C. Write JUMP instruction bit format. Show a sketch with the blocks relevant to jump instruction only.

(4+4+2)

4A. What are the different protocols used for enforcing coherence in a centralized share memory architecture? Discuss with examples.

4B. Write programming model/architecture of MSP 430 microcontroller.

4C. What are the different types of cache architecture based on its location?

(4+4+2)

5A. With a schematic diagram, show pipelined dependencies in a five – instruction sequence given below, using simplified data paths. How these dependencies are resolved via forwarding?

```
sub  $2,  $1,  $3
and  $12,  $2,  $5
or  $13,  $6,  $2
add   $14,  $2,  $2
sw  $15, 100 ( $2)
```

5B. With a diagram, explain MAC unit of a DSP Processor for two 16 bit inputs. If sum of 256 products are to be computed using MAC, with execution time 100 n sec, compute total time to complete the operation. Modify the MAC unit to prevent overflow condition. A 8 tap FIR filter with maximum sampling time = T/8. Show the implementation of the filter with necessary diagram.

5C. Describe a 4 bit Barrel left shifter with diagram and truth table.

(4+4+2)