Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

FIRST SEMESTER M.Tech. (ME) DEGREE END SEMESTER EXAMINATION
NOV 2017
SUBJECT: ADVANCED DIGITAL VLSI DESIGN (ECE - 5121)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Discuss the various options for pull-up device in an inverter and critically analyse their suitability.

1B. What is meant by switch logic and gate logic? Describe and compare them. Also show how a 4:1 mux can be implemented using switch logic that produces un-degraded outputs.

(5+5)

2A. With the help of a neat circuit diagram explain:
i) Pseudo NMOS inverter with its merits and demerits.
ii) 2 input NAND gate using BiCMOS logic indicate the function of each transistor.

2B. Explain different types of technology scaling. Illustrate the impact of full scaling on the dynamic power dissipation, Drain current and Gate capacitance.

(5+5)

3A. With the help of neat diagram, explain the process steps involved in patterning of polysilicon.

3B. In a CMOS inverter, both NMOS & PMOS transistors have W=2.0μm, L=0.5μm, process parameters k = 110 μA/V^2, V_{DD} and V_{th} are 2.2 V and 0.6V respectively. Calculate the inverter pair delay. Assume that the sheet resistance of N+ diffusion channel is 10kOhm and the electron mobility is 270 cm^2/V-sec.

3C. Implement Boolean function $F = \overline{((A+B+C)D)}$ using CMOS logic and size the transistors for optimum performance.

(5+3+2)

4A. With the help of neat diagrams explain the operations of electrically alterable and non-electrically alterable semiconductor memories.

4B. What is the word line and bit line capacitance in a 64K SRAM (256 X 256, 6 T SRAM), with access transistors of W/L ratio equal to 0.5um/0.1um ? The contacts on the bit lines are shared between pairs of cells and have a capacitance of 0.5fF each. The wire capacitance is 0.2 fF/um and the cell size is 2umX1.5um.

4C. List the limitations of 6 T SRAM and indicate remedies for the same.

(5+3+2)

5A. i) Briefly explain the design rules and compare them.
ii) For the Boolean function F(ABCD) = ((A.(B+C))+D), draw the stick diagram with and with out Euler path method.

5B. Define i) Clock skew and ii) Jitter . Also give the details of their cause and remedies.

5C. What is meant by di/dt noise? Explain with its impact in VLSI.

(5+3+2)