Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

FIRST SEMESTER M.Tech. (DEAC & MICRO) DEGREE END SEMESTER EXAMINATION
NOV 2017
SUBJECT: ANALOG AND RF VLSI DESIGN (ECE - 5102)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Derive the expression for small-signal voltage gain and output conductance for the circuit shown in **FIG. Q1A.**

1B. Obtain the expression for small-signal voltage gain and output resistance for the circuit shown in **FIG. Q1B.**

1C. Explain the effect of following as applied to current mirrors: [i] lateral diffusion [ii] oxide encroachement.

(5+3+2)

2A. [i] Consider the circuit of nMOS CG amplifier with a pMOS current source load. M_1 is the input MOS device and M_2 is the output MOS of M_2-M_3 current source circuit. Assume that the CG amplifier has a bias current of 0.1mA and that all transistors have a W/L of 100 µm/2 µm. Given that K_n = 50 µA/V^2, K_p = 17 µA/V^2, $g_{ds,n}$ = 10 µmho , $g_{ds,p}$ = 5 µmho, η = 0.1.Compute small-signal voltage gain. [ii] State the principle used in the design of RF Mixers.

2B. [i] Obtain the expression for small-signal voltage gain for the circuit shown in **FIG. Q2B** neglecting second-order effects.
[ii] Give mathematical expression for λ.

2C. Explain how a 3-MOSFET voltage divider circuit can be used to bias cascode current sink.

(5+3+2)

3A. Give the circuit of double cascode current sink. Using small signal ac model, derive the expression for output resistance. What is the minimum output voltage across the current sink? Give any one improved wide-swing cascode current mirror circuit.

3B. For the NMOS differential pair $M_{1,2}$ with a current source load formed using $M_{3,4}$, $(W/L)_{1,2}$ = 15/5, $(W/L)_{3,4}$ = 70/5, $\lambda_n = 0.06\,V^{-1}$, $\lambda_p = 0.05\,V^{-1}$. Given that $\mu_n \approx 2.5\,\mu_p$, K_p= 20 µA/V^2, $V_{DD} = -V_{SS}$ = 2.5 V, R_{bias} = 1.665 MΩ. Find the overall transconductance of the differential amplifier, differential and common-mode small-signal gain for I_{bias} = 10 µA.

3C. Give the expression for voltage gain of the circuit shown in **FIG. Q3C**. Here M_1 is biased in saturation with a drain current equal to I_1. Given that $(L/W)_1$ = 1/5 and $(L/W)_2$ = 2/1. [a] Find the voltage gain if the switch S is open. [b] What is the effect on voltage gain if the current source I_s = 0.25 I_1 is added to the circuit.

(5+3+2)

4A. [i] What do you understand by "cascode" topology? Explain the telescopic PMOS double cascode amplifier with NMOS cascode load. State the merits of the circuit.
[ii] Obtain the expression for dominant and non-dominant pole frequency for unbalanced CMOS OTA.

4B. With the circuit of PMOS based folded cascode amplifier with cascode load explain the usefulness of the same.

4C. [i] …… channel devices are used in analog design. (short/ long)
[ii] Unit of GAMMA parameter …….
[iii] Source follower is used as …… buffer. (voltage/ current)
[iv] State the condition for MOS device operated in deep-ohmic region.

(5+3+2)

5A. Explain the basic PLL block diagram with necessary analog building blocks. Sketch and explain the different waveforms of PLL in locked condition.

5B. Compare the two single stage amplifier stages shown in **FIG. Q5B.** Find the expression for small-signal voltage gain for both circuits.

5C. With a circuit of Operational Transconductance Amplifier (OTA) explain the working. How the circuit transconductance can be tuned?

(5+3+2)

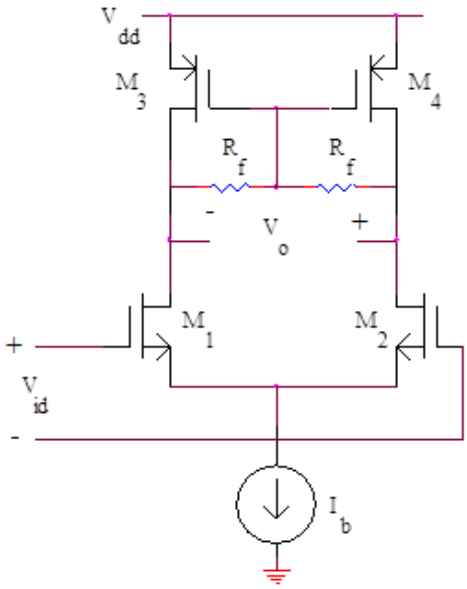


FIG. Q1A

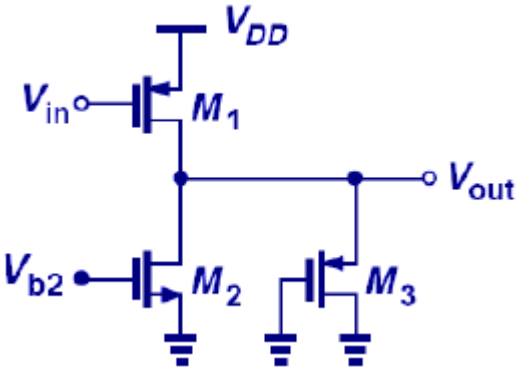


FIG. Q1B

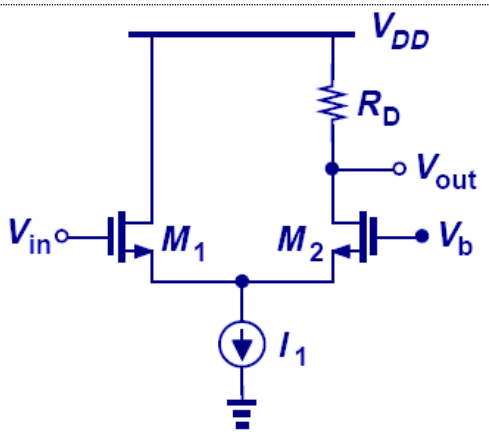


FIG. Q2B

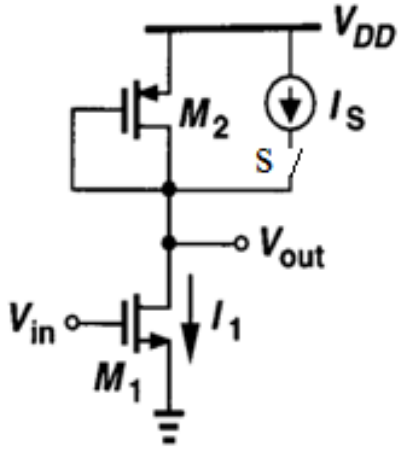
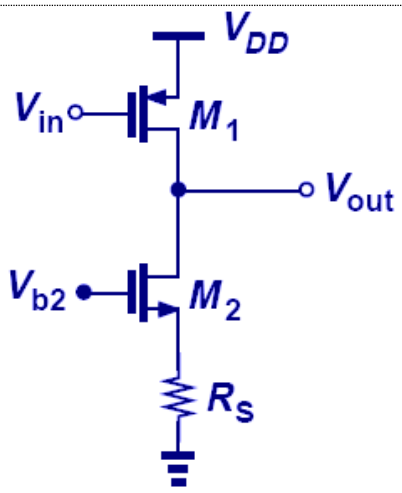
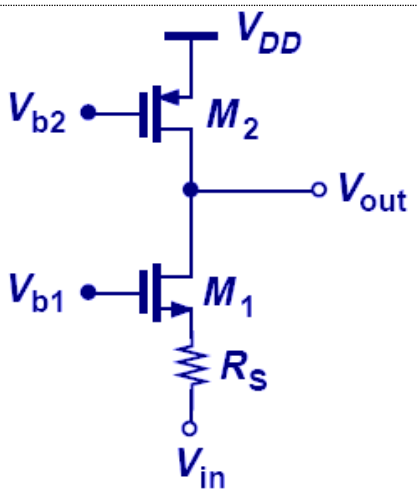


FIG. Q3C



[a]



[b]

FIG. Q5B