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# MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

*A Constituent Institution of Manipal University*

**FIRST SEMESTER M.TECH (DEAC & ME) DEGREE END SEMESTER EXAMINATION**
**NOV 2017**
**SUBJECT: PROCESSOR ARCHITECTURE & APPLICATIONS (ECE - 5103)**

**TIME: 3 HOURS** **MAX. MARKS: 50**

**Instructions to candidates**

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Describe architectural overview and on - chip memory of TMS320C64x DSP Processor.

1B. Discuss architecture and instructions of a vector register processor.

1C. Explain Interrupt based I/O strategy with algorithm / program used for implementation.

(4+4+2)

2A. A superscalar pipelined machine, capable of fetching and decoding two instructions at a time, having three functional units (F1 & F2 are 2 integer functional units + F3 is a 1 floating point). Each instruction takes one cycle to execute. Two instances of write back stages.

Given: Ten instruction code segment (I1 to I6)

- I1 requires two cycles to execute
- I3 and I4 conflict for functional unit F3
- I5 depend on value produced by I4
- I5 and I6 conflict for functional unit F2

Implement the above code using **two policies** which take maximum number of clock cycles.

2B. Write programming model/architecture of MSP 430 microcontroller and discuss it's application.

2C. Discuss structural and data dependency hazards with examples.

(4+4+2)

3A. A five stage pipeline runs following code.

I1 : lw $3, 40 ( $8)
I2: and $12, $3, $5
I3: or $13, $6, $3
I4: add $14, $3, $3
I5: sw $15, 100($3)

Only one memory (both code and data). There is a structural hazard any time fetching an instruction and access data are in the same cycle. The hazard must be resolved in favor of the instruction that access data.

Identify data dependencies in the given code.

Draw two schematics

i) One showing dependencies

ii) Other showing appropriate methods to overcome hazards.

What is the total execution time?

3B. What are the taxonomy of parallel processor architectures? Explain. Also discuss processor interconnect strategy for different memory architectures.

3C. Interface 2K byte RAM using address decoder and other logic circuits at starting address 0000F800H.

(4+4+2)

4A. Discuss compiler based solution to enforce coherence in a centralized shared memory architecture. Two processors A and B are connected to a enforce memory. Initial content of memory location M is FFH. CPU A reads the content of memory location M and then writes 00 to M. With the help of different protocols, narrate the bus activities and updating of contents in caches of different processors.

4B. A scheme for MIPS that uses ALU for implementing all basic instructions instead of adders. With brief explanation and diagram, show how this is implemented with necessary control signals.

4C. Consider the following two cache memory configurations

a) 8 KB I & D cache.

Instruction miss rate = 0.64%. Data miss rate = 6.47%.
Hit time = 1. Miss time = 50.
75% accesses are from instructions.

b) 16KB unified cache.

Aggregate miss rate = 1.99%.
Hit time = 1. Miss rate = 50.
75 % accesses are from instructions. Data hit has 1 stall.
Find AMAT for both. Which one is better?

(4+4+2)

5A. With necessary sketches, explain mechanism to maximize set associativity and reduction in probability of thrashing used in ARM 940T.

5B. How valid translations in page tables happen in ARM MMU. Explain all methods with necessary diagrams.

5C. Discuss overflow / underflow solutions associated with MAC unit in a DSP Processor.

(4+4+2)