Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

I SEMESTER M.TECH. (INDUSTRIAL AUTOMATION AND ROBOTICS)

END SEMESTER EXAMINATIONS, NOV 2017

SUBJECT: ANALOG AND DIGITAL ELECTRONICS [MTE 5131]

REVISED CREDIT SYSTEM
(21/11/2017)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ANY FIVE FULL** questions.
- Data not provided may be suitably assumed

1A.	INDRA is a low level radar to search and track low flying cruise missiles, helicopters and aircraft for the Indian Army. It uses a circuit to fix the DC level of an AC waveform to a specific value which is based upon the application of the waveform. Design a circuit using an Op-Amp, which would perform this operation and describe its working using a suitable waveform.	**05**
1B.	Analyze the output of the clocked sequential circuit shown in figure 1B.	**05**
2A.	With a suitable diagram describe the architecture and working of the Xilinx XC 3020 Logic Cell Array, CLB.	**05**
2B.	Figure 2 B illustrates an Audio mixer which uses two or more signals as inputs to it and adds them to appear at the output. Design such a circuit using an Op-Amp.	**05**
3A.	Design a PAL for the following expressions: $X(A,B,C,D) = \Sigma m(1,3,5,7,8,9,11)$ $Y(A,B,C,D) = \Sigma m(0,2,4,5,7,8,10,11,12)$	**05**
3B.	A UHF-radar operates in the C-band of frequencies which ranges from 300 MHz to 1 GHz. A C-band signal generator is used as an input to the transmission system and it generates frequencies within the range of 200 MHz to 1.5 GHz. Design a filter to pass the range of frequencies of 500 MHz to 700 MHz through the transmitting antenna for this system.	**05**
4A.	Describe the design and implementation of a high pass filter used in studio recording and sound reinforcement to attenuate extraneous low frequency content like mechanical rumble and voice plosives.	**05**
4B.	With a suitable sketch explain the functioning of a memory cell in the Xilinx XC 3020 CLB.	**02**
4C.	Differentiate between the F, FG and FGM modes of operation of the Xilinx XC 3020 CLB.	**03**
5A.	Describe the construction of a 4 x 1 Multiplexer and a 1 x 4 Demultiplexer.	**02**

5B.	Give reasons for the superior operation of a Priority encoder over a normal encoder.	**03**
5C.	Design a ROM to find the square of a 3-bit number.	**05**
6A.	Design a 3 bit Gray to Binary code converter.	**06**
6B.	Reduce the state diagram shown in figure 6B.	**04**

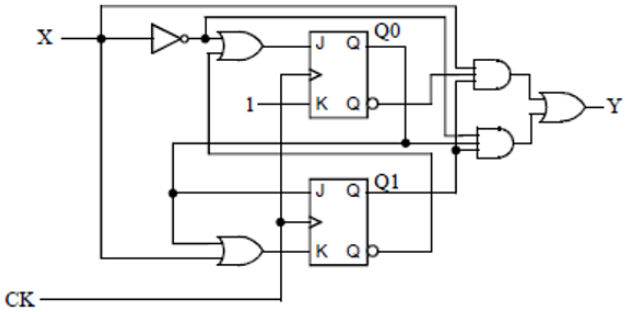

Figure 1 B

Figure 2 B

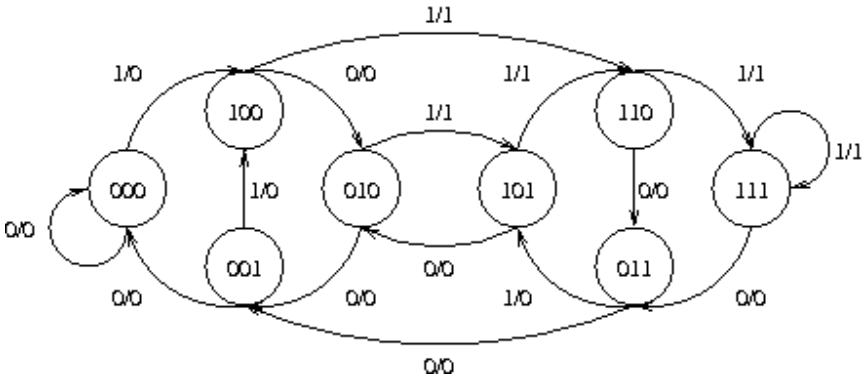

Figure 6 B