Question Paper

MANIPAL UNIVERSITY

SCHOOL OF INFORMATION SCIENCES
SECOND SEMESTER MASTER OF ENGINEERING - ME (Embedded Systems)
DEGREE EXAMINATION - NOVEMBER 2017
DATE : Wednesday, November 15, 2017
TIME : 10:00AM - 1:00PM
Digital Signal Processing [ESD 602]

Marks: 100   Duration: 180 mins.

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Answer all the questions.

1)   Using Radix-2 DIF-FFT algorithm, compute the IDFT. Given   (10)
      that
      X(k) = [20, -5.828-j2.414, 0, -0.172-j0.414, 0, -
      0.172+j0.414, 0, -5.828+j2.414].

2)   Prove that an FIR filter having symmetric response   (10)
      provides a linear phase. Show the realization.

3)   Obtain the frequency sampling structure of an FIR filter   (10)
      having N number of filter coefficients.

4)   Determine the parameters of FIR filter using windows   (10)
      which has the following specifications, ω_p = 0.2π rad, ω_s =
      0.3π rad and stop-band attenuation is 50 dB

5)   A lowpass filter is to have magnitude response constant   (20)
      within -1dB in the frequency range 0 to 100Hz. Response
      should fall monotonically to less than -15dB at frequency
      of 150Hz. Design a digital Chebychev filter using bilinear
      transformation to meet the above specifications. Sampling
      period is 1mSec. Realize the filter.

6)   What is Multirate Signal Processing? Obtain the   (10)
      expressions both in time domain and frequency domain for
      the signal, whose sampling rate is changed by a rational
      factor I/D.

7)   What is a digital filter bank? Explain how an uniform DFT   (10)
      filter bank can be implemented using multirate signal
      processing.

8)   Explain LMS adaptive algorithm. Explain how LMS adaptive   (10)
      algorithm is made use to make the Weiner Filter
      Configuration adaptive based on the steepest descent

technique.

9) Explain how a higher throughput is obtained using the VLIW architecture. Give an example of a DSP that has VLIW architecture. Explain what is meant by instruction pipelining. Explain with an example, how pipelining increases the throughput efficiency. (10)

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