Question Paper

Exam Date & Time: 08-Jan-2018 (10:00 AM - 01:00 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

SCHOOL OF INFORMATION SCIENCES
FIRST SEMESTER MASTER OF ENGINEERING - ME (VLSI Design)
DEGREE EXAMINATION (MAKE - UP) - JANUARY 2018
DATE : MONDAY, JANUARY 08, 2018
TIME : 10:00AM - 1:00PM

Digital Systems and VLSI Design [EDA 613]

Marks: 100 **Duration: 180 mins.**

Answer all the questions.

1)	a) Briefly give the basic structure of Amorphous materials, Polycrystals and Single crystals. b) Write short notes on crystal defects.	(10)
2)	Explain, with a neat diagram, horizontal tube furnace system and its various sections used in thermal oxidation method.	(10)
3)	Compare positive and negative photoresists.	(10)
4)	Explain the deposition process steps.	(10)
5)	With diagrams, compare NELT, NELS and HMOS static load inverters.	(10)
6)	Derive an expression for the switching power dissipation component in a CMOS circuit. Discuss methods to reduce this component by analyzing each element in this expression.	(10)
7)	What is transistor sizing? What is its importance? Explain the T-sizing of the following Boolean expression: Z = ((A.B + C) D)'	(10)
8)	What are the various components of parasitic capacitances that show up at high frequencies? Show them in the low frequency, small signal model.	(10)
9)	Design a fully complimentary single bit full adder using minimum number of transistors. Using this adder, explain how do you construct an adder/subtractor circuit.	(10)
10)	How do you automate the complex logic gates layout? Explain this algorithm, with examples, which uses Euler path.	(10)

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