Question Paper

MANIPAL UNIVERSITY

SCHOOL OF INFORMATION SCIENCES
FIRST SEMESTER Master of Engineering - ME (VLSI DESIGN)
DEGREE EXAMINATION - NOVEMBER 2017
DATE : Thursday, November 16, 2017
TIME : 10:00AM - 1:00PM
High Level Digital Design [EDA 611]

Marks: 100 **Duration: 180 mins.**

Answer all the questions.

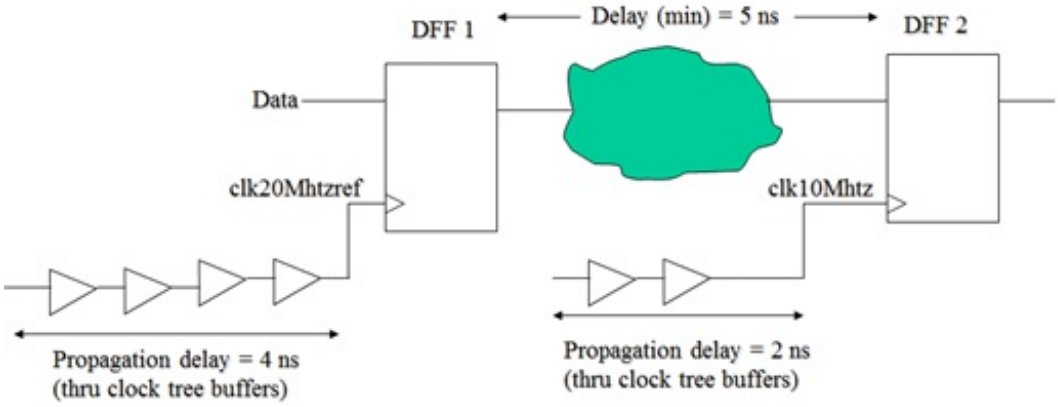
1) What is VLSI design flow? Explain with a flowchart. (10)

2) Solve the logic equation F(a,b,c,d)=Σ(0, 1, 5, 7, 8, 10, 14, 15) (10)

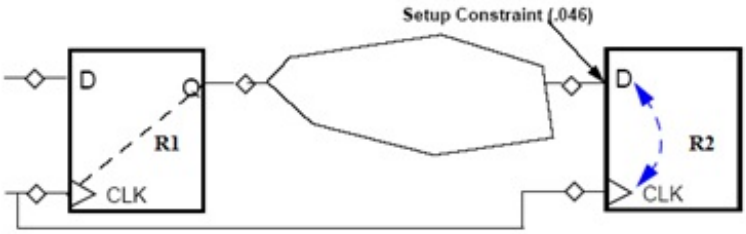
3) Design a Moore machine with an example (10)

4) Explain Static Timing Analysis (STA) with necessary diagram & equations (10)

5) Detect the timing violation with neat timing diagram for the following design. Consider the following Clock skew of 3.72 between clk20Mhzref and clk10Mhz & clock network delay (10)



6) Draw the timing diagram for the given design & calculate the setup slack (10)



R1 Source Clock signal timing parameters:
Clock Edge = 2.002 ns
Clock path delay = 0.002 ns

Data path delay = 13.002 ns
Setup time constraint = 0.046 ns

R2 Destination Clock signal timing parameters:
Min Edge = 20.02 ns
Min clock path delay = 0.500 ns

7) Design synchronous FIFO using dual port memory (10)

8) Explain in detail Logic Array Block (LAB) with neat diagram (10)

9) Explain features of AMBA AHB bus and its components (10)

10) What is the burst & wrap operation in AMBA bus explain with necessary timing diagram (10)

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