Question Paper

MANIPAL UNIVERSITY

SCHOOL OF INFORMATION SCIENCES
FIRST SEMESTER MASTER OF ENGINEERING - ME (VLSI DESIGN)
DEGREE EXAMINATION - NOVEMBER 2017
DATE : Saturday, November 18, 2017
TIME : 10:00AM - 1:00PM

System on Chip Design [EDA 615.5]

Marks: 100 **Duration: 180 mins.**

Answer all the questions.

1) Give the flow diagram of System-on-a-chip design and explain the basic SoC System Model (10)

2) Explain the Hardware/Software codesign with an example. Illustrate hardware/software codesign space for given an application (10)

3) Explain Specification & modeling and Pre-partitioning analysis in an Electronic System Level Flow (10)

4) Describe the generic template for the System on Chip application (10)

5) Explain branch target buffers. Describe static and dynamic branch predictions (10)

6) State the dependencies in instructions shown below. Show and describe the timing for a dataflow with three separate floating point unit and single floating point instructions. The adder unit, multiply unit and divider unit takes 2, 4 and 6 clock cycles to complete their operations respectively. (10)

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ADD R6, R2, R1
MUL R8, R3, R5
DIV R4, R6, R8
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7) a) What is Transaction Lookaside Buffer(TLB)? Explain the address translation with the help of a neat block diagram. (10)
b) Determine the average access time assuming a TLB hit ration of 0.8 with the following specification
Number of entries in the TLB = 8
Time taken to conduct an associative search in the TLB = 100 ns
Main memory access time = 900 ns

8)	a) Explain the write policies of cache with neat diagrams b) What are the strategies for line replacement at Miss Time in cache organization?	(10)
9)	Explain the criteria for choosing the suitable interconnect architecture	(10)
10)	Describe the various Hardware/Software Interfaces with examples	(10)

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