Question Paper

MANIPAL UNIVERSITY

SCHOOL OF INFORMATION SCIENCES
FIRST SEMESTER MASTER OF ENGINEERING - ME (VLSI DESIGN)
DEGREE EXAMINATION - NOVEMBER 2017
DATE : Tuesday, November 21, 2017
TIME : 10:00AM - 1:00PM
Verification [EDA 617]

Marks: 100 **Duration: 180 mins.**

A

Answer all the questions.

1) Explain the following commonly used terminology in verification: (10)

- (a) SoC
- (b) BFM
- (c) Regression
- (d) Constrained Random Verification

2) Explain with examples about the following SystemVerilog data types: (10)

- (a) Enumerated
- (b) Dynamic arrays
- (c) Unions
- (d) Queues
- (e) Logic

3) Explain the difference between shallow copy and deep copy operations. Give examples with descriptive diagrams to substantiate your answer. (10)

4) Write the output of the following code segment (10)

```
module test();

class A;
randint y;
constraintplk {y > 2*2*2; y < 7;}
endclass

class B extends A;
```

```
constraintplk {y > 5; y < 7;}
endclass

class C extends B;
constraintrpr {y > 3; y < 7;}
endclass

A a;
B b;
C c;

initial
begin
a=new();
b=new();
c=new();

if(a.randomize() == 1)
    $display("(1) y=%0d",a.y);
else
    $display("(1) Randomization Failure");
if(b.randomize() == 1)
    $display("(2) y=%0d",b.y);
else
    $display("(2) Randomization Failure");
if(c.randomize() == 1)
    $display("(3) y=%0d",c.y);
else
    $display("(3) Randomization Failure");
end

endmodule
```

5) Can the following scenarios occur? Give examples that substantiate your answer. (10)

1. (a) 100% code coverage of a design has been achieved, but not 100% functional coverage.
2. (b) 100% functional coverage of a design has been achieved, but not 100% code coverage.

6) A) Define a cover group 'mcg' with a cover point 'mrngkind' (10)

using bin definitions as :
a) 'zerobin' {0}
b) 'lobin' {{1:4}, 10}
c) 'hibin' {9:$}
d) 'miscbin' - the rest of values
where, 'mrngkind' is a bit-vector with range [0:15].
(5 marks)

B) What is the need for verification? (5 marks)

7) Write the output of the following code segment: (10)

```
program test;

task print(intdisplayvar);
  $display("%0d", displayvar);
endtask

initial
begin
for(inti=0;i<5;i++)
begin
int j;
   j = i;
fork
print(j);
join_none
end
wait fork;
end

endprogram
```

8) Write (code) a concurrent assertion in SystemVerilog to: (10)

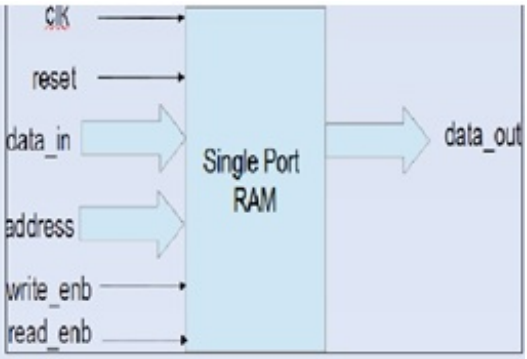
check whether a signal '**mysig**' goes high at any random point of time during the entire simulation.

The other signal names of interest while writing this assertion are '**clk**' and '**reset**'.

9) Write out the verification plan for a single-port RAM, the specifications of which are as follows: (10)

The key features of the RAM are as follows:

- The design is a single port RAM
- The RAM clock frequency is 50 MHz
- The depth of the RAM is 32 locations
- The data width is 8-bits
- Changes in the RAM happen at positive edge of clock
- Synchronous active high reset. On assertion, the data output becomes 'z'
- The write operation into the RAM is supported. For invalid address, the RAM does nothing
- The read operation from the RAM is supported. For invalid address, i.e., address value > that supported by the address width, the invalid address is truncated to fit in the address width and the data read from the RAM will be done using that truncated location
- The RAM does not support simultaneous (concurrent) read and write operations



Include all scenarios that you can think of, including corner cases in your verification plan.

10) Code ONLY the **monitor** module of the testbench for the single-port RAM, the specifications of which are already given in question number 10. (10)

-----End-----