Question Paper

MANIPAL UNIVERSITY

SCHOOL OF INFORMATION SCIENCES
SECOND SEMESTER MASTER OF ENGINEERING - ME (VLSI DESIGN)
DEGREE EXAMINATION - NOVEMBER 2017
DATE : Wednesday, November 15, 2017
TIME : 10:00AM - 1:00PM

Advanced VLSI Design [EDA 604]

Marks: 100 **Duration: 180 mins.**

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Answer all the questions.

1) a) Explain the effect of Temperature and Voltage on CMOS Resistor. (10)
b) Estimate the minimum and maximum resistance of an n-well resistor with a length of 100 μm and a width of 10Âμm over a temperature range of 0 to 100Â°C.
[Data Given: TCR = 10,000ppm/^{o}C; N-well sheet resistance = 2KΩ to 3KΩ/square]

2) Starting from a general 2-port network, derive a complete low frequency, small signal model for a MOSFET. (10)

3) a) List the applications of a current source / current mirror. (10)
b) Design four current sinks with values 20, 30, 50 and 70 μA. What is the minimum voltage across each current sink? Assume V_{DD} = +5V and V_{SS} = 0V. Make necessary assumptions.

4) With a diagram, explain **cascode current mirror**. What are its advantages over a simple current mirror? (10)

5) a) What are the different performance parameters of an amplifier? Show the dependencies among them using ***'analog design octagon'***. (10)
b) What are the three amplifier topologies? Compare them as far as voltage-gain, input impedance and output impedance are concerned.

6) With the help of a small-signal equivalent circuit, obtain the expression for $\mathbf{A_v}$ for a CMOS Common-Gate amplifier with passive resistor load. Assume finite output impedance, r_0 and signal source impedance R_s. (10)

7)	Explain, with the help of a neat schematic diagram, a bandgap voltage reference. What are the advantages of this circuit over other simple references?	(10)
8)	What is Common Mode Rejection Ratio (CMRR) of a differential amplifier? Explain the diagram used to measure it?	(10)
9)	With relevant diagrams, explain the working of Current Steering DAC. Derive an expression for its $\|INL\|_{max}$ and $\|DNL\|_{max}$.	(10)
10)	With the help of a block schematic, explain a Single Slope Integrating ADC. What are the accuracy issues related to it?	(10)

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