Question Paper

MANIPAL UNIVERSITY

SCHOOL OF INFORMATION SCIENCES
FIRST SEMESTER MASTER OF ENGINEERING - ME (VLSI DESIGN)
DEGREE EXAMINATION - NOVEMBER 2017
DATE : Tuesday, November 21, 2017
TIME : 10:00AM - 1:00PM

Low Power VLSI Design [EDA 608]

Marks: 100 **Duration: 180 mins.**

Answer all the questions.

1)	List power dissipation components in digital CMOS circuits and explain	(10)
2)	Model the junction Capacitance in CMOS with neat diagram and discuss	(10)
3)	Discuss briefly the following (5 + 5) a) VTCMOS b) Stack Effect	(10)
4)	Design and explain high to low level shifter	(10)
5)	List the rules to be followed placing the level shifter in multi-voltage domain and briefly discuss the pitfalls and how it is overcome.	(10)
6)	Discuss the dynamic and leakage power profiles and how it impacts on power gating	(10)
7)	Explain the significance of header and footer fabric in power gating	(10)
8)	How retention register is used to save power and discuss	(10)
9)	Design and draw the necessary waveform for the power control sequence without retention	(10)
10)	Discuss the dynamic voltage and frequency scaling	(10)

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