Question Paper

MANIPAL UNIVERSITY

SCHOOL OF INFORMATION SCIENCES
SECOND SEMESTER Master of Engineering - ME (VLSI DESIGN)
DEGREE EXAMINATION - NOVEMBER 2017
DATE : Thursday, November 16, 2017
TIME : 10:00AM - 1:00PM

Physical Design [EDA 616.8]

Marks: 100 **Duration: 180 mins.**

Answer all the questions.

1)	State and explain the four design approaches for reducing the delay of large fan-in circuits	(10)
2)	Explain the four types of data required in Floorplanning	(10)
3)	Explain clock planning in VLSI Floorplanning	(10)
4)	What are the goals and challenges of VLSI placements? Define Standard Cells, Macro Cells and Spare Cells.	(10)
5)	What are load based and gain based optimizations?	(10)
6)	State any five wire estimation methods and explain them briefly	(10)
7)	What are the advantages of modeling physical faults as logical faults? List and briefly explain different types of fault models	(10)
8)	Explain the importance of testing in VLSI. Find out the probability of a faulty chip which consists of 10^8 transistors with the probability of a faulty transistor is 10^{-6}	(10)
9)	Explain forward implication, backward implication, justification and backtracking with examples	(10)
10)	What is the significance of LFSRs? Explain a 4 bit LFSR with 0000 state	(10)

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