Question Paper

MANIPAL UNIVERSITY

SCHOOL OF INFORMATION SCIENCES
SECOND SEMESTER MASTER OFM ENGINEERING - ME (VLSI DESIGN)
DEGREE EXAMINATION - NOVEMBER 2017
DATE : Saturday, November 18, 2017
TIME : 10:00AM - 1:00PM

Universal Verification Methodology [EDA 610]

Marks: 100 **Duration: 180 mins.**

Answer all the questions.

1)	Explain the functionality of following components with example. a. Monitor b. Scenerio Generator	(10)
2)	Explain Arrays in SystemVerilog.	(10)
3)	Explain the functionality of following with example (5+5=10 Marks) a. Encapsulation b. Polymorphism	(10)
4)	Explain the functionality of following with example (5+5=10 Marks) a. uvm_object class b. uvm_component class	(10)
5)	Explain the functionality of following (5+5=10 Marks) a. Block level environment b. Integration level environment	(10)
6)	Explain different components in UVM Testbench.	(10)
7)	Illustrate UVM Factory coding convention 2 and convention 3 with example.	(10)
8)	Explain about UVM factory overrides.	(10)
9)	Write a note on creation of transaction using uvm_sequence with an example.	(10)
10)	Explain the functionality of uvm_driver with example.	(10)

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