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MANIPAL INSTITUTE OF TECHNOLOGY
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**V SEMESTER B.TECH (COMPUTER SCIENCE AND ENGINEERING)**
**MAKE-UP EXAMINATIONS, Dec 2017/Jan 2018**
SUBJECT: **COMPUTER ARCHITECTURE [CSE 3101]**
**REVISED CREDIT SYSTEM**

Time: 3 Hours 19-12-2017 MAX. MARKS: 50

**Instructions to Candidates:**

- Answer **ALL** the questions.
- Missing data, if any, may be suitably assumed.

**1A.** Briefly explain the different programmatic levels of parallel processing. Explain how the computer system is characterized according to Handler? **4M**

**1B.** Design a pipeline that adds two normalized floating point numbers A = a $x$ $2^p$ and B=b $x$ $2^q$ where a and b are fractions and p and q are their exponents respectively. What are the operations performed by the different stages of this pipeline? **4M**

**1C.** With the help of a neat diagram explain the sub cycle that happens immediately after the instruction *j* is fetched into the system.

```
i:  DADDU  R1, R2, R3
j:  INT 21h            ; interrupt service routine starts from address m
k:  SD R4, 0(R1)
```
**2M**

**2A.** Consider the following pipelined processor with 5 stages in figure 2A. It has a total evaluation time of 6 clock cycles. All successor stages must be used after each clock cycle.

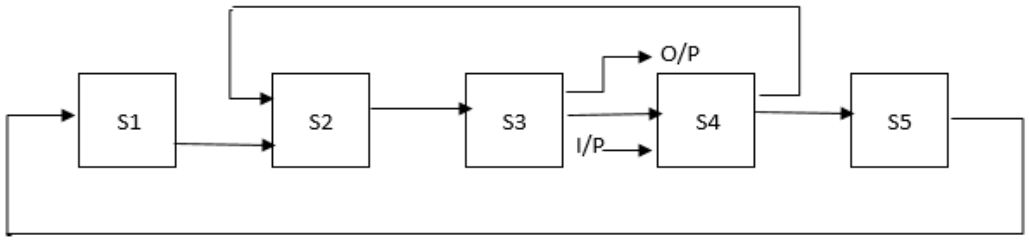


Figure 2A

i. Draw the reservation table for the above and find out the collision vector
ii. Draw the state transition diagram which shows all possible latency cycles
iii. List all simple cycles and greedy cycles
iv. Calculate the MAL and efficiency of this pipeline **3M**

**2B.** What are the different data hazards introduced due to out-of-order execution of the following code sequence and demonstrate how to resolve them?

```
A:  L.D      F0, 0(R1)
B:  MUL.D    F4, F0, F2
C:  S.D      F4, 0(R1)
E:  L.D      F0, 0(R1)
F:  MUL.D    F4, F0, F2
G:  S.D      F4, 0(R1)
```
**3M**

**2C.** With a neat diagram briefly explain the Illiac-IV computer configuration. Write the algorithm to find the sum of even numbers from 1 to 12 using an array of 8 processing elements in an SIMD machine. Write the masking scheme for the data routing. **4M**

**3A.** Write the routing functions of Barrel Shifter and Mesh Connected Illiac Network. Prove that an Illiac routing functions are a subset of Barrel shifting functions by taking N number of PEs such that, $5 < N < 50$. Write all the permutation cycles for this. How will you relate the connectivity of these two networks? With the help of the above permutation cycles prove this relation. **5M**

**3B.** Design an Omega Network which has 4 switch boxes in each stage. Clearly show all the routing functions by considering all the PEs. Show the switch settings in the above design for routing a message from $PE_0$ to node $PE_6$. Find another source and destination which creates a block in the above path in the second stage. Show the switch settings for this in the same design. **3M**

**3C.** Explain how the cluster middleware is responsible for enhancing availability of the cluster? **2M**

**4A.** What is cache coherence problem? Discuss briefly how the software cache coherence schemes work. Also write the merits and demerits of them. **3M**

**4B.** A SMP system contains three processors with L2 caches connected using a time shared bus is shown in the figure 4B. Explain how the following cases are handled in the initiating processor and the snooping processors that uses MESI protocol for the scenario given below. Draw the state transition diagram for both cases.

i)Processor A wants to modify the value of Z to 100

ii) Processor B wants to modify the value of X to 50

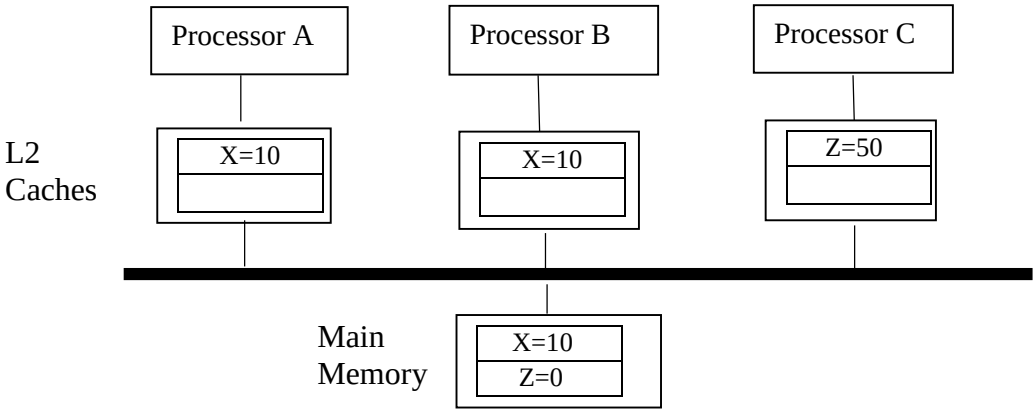


Figure 4B **4M**

**4C.** Define Process and Thread in the context of multithreaded processors. With the help of diagrams explain the different approaches to multithreaded processors that have hardware for issuing multiple instructions per cycle and simultaneous execution of multiple threads in a cycle. **3M**

**5A.** Draw a neat diagram of Intel Core Duo. Explain the features provided in this product to handle the following:

i) Chip heat dissipation ii) Inter-processor interrupts **4M**

**5B.** Explain briefly any three classes of applications that benefit directly from the ability to scale throughput with the number of cores. What are the advantages of a shared L2 cache on the chip over dedicated caches? **4M**

**5C.** With a neat diagram briefly explain the shared disk approach in the clusters. Write its benefits and limitations. **2M**