Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

V SEMESTER B.TECH. (COMPUTER SCIENCE AND ENGINEERING)

END SEMESTER EXAMINATIONS, NOVEMBER 2017

SUBJECT: COMPUTER ARCHITECTURE [CSE 3101]

REVISED CREDIT SYSTEM
(15/11/2017)

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Showing the spaces of data, information, knowledge and intelligence from the viewpoint of computer processing, explain the relationship between them. **4M**

1B. Derive the expressions for speedup, efficiency and throughput of a k-stage linear pipeline processor in terms of the number of tasks n and the pipeline stages k. What is the speedup, efficiency and throughput as $n \rightarrow \infty$? **4M**

1C. A processor is executing a program with P instructions. The i^{th} instruction is a memory read instruction, the right-most N bits of which is a memory reference that contains the address of the operand to be read. With neat diagrams explain the data flow that take place in the processor to fetch the instruction and the operand for the i^{th} instruction execution. **2M**

2A. Design a 4-stage linear pipelined floating point adder to add two floating point numbers $A = a \times 2^p$ and $B = b \times 2^q$. Write the operations performed in each stage. **3M**

2B The routing functions of a Shuffle-Exchange network with N PEs are defined as follows:

$$S(a_{n-1} \ldots\ldots a_1 a_0) = \overline{a_0} a_{n-1} \ldots\ldots a_1$$
$$E(a_{n-1} \ldots\ldots a_1 a_0) = \overline{a_{n-1}} \ldots\ldots a_1 a_0$$

where $a_{n-1} \ldots\ldots a_1 a_0$ is a PE address and $n = \log_2 N$

Write the permutation cycles of both the routing functions and draw the recirculating network for N=16. **3M**

2C. What do you mean by masking schemes in SIMD array processor? Explain.
Assume that an N × N matrix is stored in SIMD processor such that column i is stored in the consecutive locations staring from address 100 in PEMi. What should be the global index register and local index register values to access each row and principal diagonal elements of the matrix? Briefly explain.
Write the SIMD algorithm to find the sum of each column. **4M**

3A. A multiprocessor system consists of three processors A, B and C and uses MESI protocol for cache coherence. Initially the cache line in all these processors are empty. The following sequence of operations take place on the memory location x: A reads x, C reads x, C writes x, A reads x, B reads x, B writes x. Tabulate the state of the cache line in all the processors at the end of each processor action in the following format

Processor Action	State in A	State in B	State in C
A reads x			
C reads x			
C writes x			
A reads x			
B reads x			
B writes x			

Explain how cache coherence is achieved when each of the above operations take place. **5M**

3B. With a neat diagram for each, explain the approaches to execute multiple instructions either from a single thread or from multiple threads in pipeline architectures. **5M**

4A. Write the variables in a multicore organization. With neat diagrams explain the general organizations for multicore systems. **5M**

4B. Compare the active secondary clustering methods along with their benefits and limitations. **3M**

4C. Explain write update and write invalidate protocols to solve cache coherence problem in multiprocessor systems. **2M**

5A. Explain parallelizing computation techniques used in clusters. Also explain the cluster middleware services that enhance the availability of the cluster. **5M**

5B. Which are the PEs directly connected to PE_0 in an Illiac network and PM2I network with N=16. Using this information prove that the connectivity in a PM2I network is increased from the Illiac network by having $(2n-5)2^{n-1}$ more direct links **3M**

5C. List any four advantages of L2 cache on the chip in the multicore processors over dedicated caches **2M**