Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

FIFTH SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION
NOV/DEC 2017
SUBJECT: COMPUTER ORGANIZATION AND ARCHITECTURE (ECE - 3106)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Draw the accumulator based and stack based machines. Write optimized code for accumulator based and stack based machine for evaluating the following expression. $Y = \frac{A+B-C}{D} * (E + F)$. The machine has 32 registers, 32kbytes of memory and it can support 32 operations. Assume A, B, C, D, E and F are memory locations.

1B. The data source contains a set of five different symbols with the corresponding frequencies as given in table below. Encode these symbols using Huffman's encoding technique and calculate the efficiency.

Symbol	Frequency
A	24
B	12
C	10
D	8
E	8

1C. Write the different types of program control instructions with suitable example.

(5+3+2)

2A. Derive carry look ahead equations and design a 16-bit adder using 4 bit carry look ahead(CLA's). Also calculate the worst case adder time of this 16-bit adder.

2B. Perform multiplication of 46 X 59 using i) Unsigned sequential multiplier by showing all the iterations. ii) Bit pair recoding method, assuming the numbers are positive.

2C. Draw the Wallace tree structure for 7 single bit operand CSA. Write the expression for finding the number of CSA levels for the above Wallace structure

(5+3+2)

3A. Design a micro programmed control unit for Booth's multiplier by giving the RTL code. Explain the control memory organization of Booth's multiplier with a neat diagram.

3B. Design a 4 bit general purpose register for the truth table shown below

S1	**S0**	**CLR**	**Function**
X	X	1	Clear output
0	0	0	Increment
0	1	0	Rotate right
1	0	0	Arithmetic right shift
1	1	0	Rotate left

3C. Build a hardware to implement the following: (Assume A, B, X are 4 bit registers)

If A= B and X ≠ zero then A ← A+B
else A ← A - B

(5+3+2)

4A. With the relevant diagrams explain the various cache memory mapping techniques. Consider the hexadecimal main memory address DACB9876 and size of the cache is 64KB. Assume line (block) size is 256 Bytes. Find the i) cache line address and word address in direct mapping. i) set address and the Tag address if 4 lines are made as one set (4 blocks per set).

4B. Explain the following in brief : i) Programmed I/O ii) Interrupt I/O iii) DMA

4C. The access time of a cache memory is 50 ns and that of the main memory is 500 ns. It is estimated that 80% of the main memory requests are for read and the remaining are for write. The hit ratio for read access only is 0.9 and a write-through policy is used.

i) Find the average access time considering only the read cycles.
ii) What is the average time if the write requests are also taken into consideration?

(5+3+2)

5A. Describe the following architectures i) RISC ii) CISC iii) VLIW

5B. Derive the expression for finding the average number of instructions executed per instruction cycle in a pipeline organization. Consider 25% of the instructions are branch instructions, compute the average number of instructions computed per instruction cycle in a 5 stage pipeline organization.

5C. Explain the operation of i) Circular ii) Bit reversed addressing modes in Digital signal processors.

(5+3+2)