Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

FIFTH SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION
NOV 2017
SUBJECT: COMPUTER ORGANIZATION AND ARCHITECTURE (ECE - 3106)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Draw the organization of register based, accumulator based and stack based machines. For the expression G=(A+B*C)/(D-E*F), write the optimized code for all the above machines.

1B. Encode the following instructions using Huffman encoding technique, given are the instructions and their frequency of usage. Calculate the percentage of redundancy.

Instruction	Frequency of usage
MOV	0.22
CALL	0.12
RET	0.13
ADD	0.09
AND	0.07
CMP	0.06
JMP	0.08
MUL	0.09
DIV	0.04
SUB	0.1

1C. A computer instruction set supports the following Boolean instructions:
XOR Y,X; Y← X XOR Y
AND Y,X; Y←X AND Y.
Write how to perform Y← X OR Y using the above two instructions.

(5+3+2)

2A. Draw the flowchart for the restoring division algorithm. Give the block diagram of a trial processing unit for the above algorithm. For the function table given below, design a 4 bit general register.

S1	**S0**	**Function**
0	0	Clear
0	1	Decrement
1	0	Shift left
1	1	Load external data

2B. Perform multiplication on -46 X 59 using Booth's algorithm. Show all the iterations. Verify your answer using Bit pair recoding method. Write how many iterations may be needed in the second method?

2C. Assume the CSA add time is half of the CPA time. Calculate the total time required to add, by giving suitable expressions in a fully parallel 16 operand summation. Find the number of guard bits required. If a Wallace structure is used what will be the total time taken?

(5+3+2)

3A. Show the processing section with various control signals and then design a Hardwired Control circuit using counter, decoder and PLA for the following algorithm by giving the state diagram:

Declare registers A[8],B[8],C[3], Inbus [8], Outbus[8];
START: A← 0, B←Inbus, L←4;
LOOP:A←A+B,C←C-1;
If C< > 0 then go to LOOP
Outbus←A;
HALT: Go to HALT

3B. Design an Arithmetic unit for the following specifications: A and B are 4 bit data.

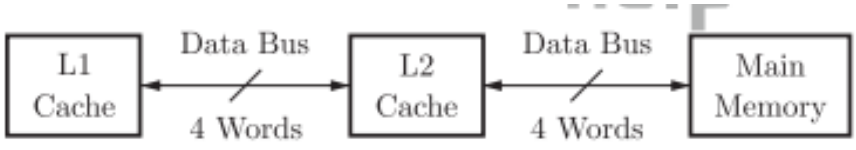
S1 S0	F
0 0	A+B
0 1	INC B
1 0	Shift left A
1 1	DEC A

3C. Draw the various bus organization structures and write how the speed of instruction execution improves with a suitable example

(5+3+2)

4A. What are the different ways to handle multiple interrupts from several I/O devices? Explain each technique with neat sketches and example.

4B. A CPU uses two cache memories L1, L2 where it can have direct access with L1. The memory access times are 2 nanoseconds, 20 nanoseconds and 200 nanoseconds for L1 cache, L2 cache and main memory unit respectively. If the hit ratios of L1, L2 are 0.9, 0.99 respectively, find the Total average access time if only read cycles are considered.



4C. Give the diagram that converts the logical address in to its equivalent physical address based on the virtual memory concepts in paging.

(5+3+2)

5A. Discuss the various pipeline hazards in brief. In a 5 stage pipeline organization, for the given set of instructions draw the pipeline diagram by identifying the hazard. Optimize the code to give improvised pipeline diagram.

Address	Instruction
101	ADD r1, r2
102	MOV r3, r1
103	JMP 101
104	DEC r4

5B. Explain the following architectures i) VLIW ii) RISC

5C. A DSP has a circular buffer with start and end addresses as 0200h and 020Fh, respectively. What would be the new values of address pointer of the buffer if, in the course of address computation, it gets updated to i) 0212h , ii) 01FCh ?

(5+3+2)