Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

FIFTH SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION
NOV/DEC 2017
SUBJECT: MICROCONTROLLERS (ECE -3102)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. With a neat block diagram, explain the programming model of 8051.

1B. Explain the memory organization of 8051 with a neat diagram.

1C. Explain DIV instruction with an example.

(5+3+2)

2A. Write a program for 8051 to find the sum of 20, 8-bit unsigned numbers stored in the array starting from 7000H onwards in data memory. Store the result at 8050H onwards in data memory. Place your code at E000H onwards.

2B. Explain the following addressing modes and illustrate with one example:

a. Immediate addressing b. Register indirect addressing c. Direct addressing

2C. Explain the functions of the following pins of 8051MC. Mention the direction of each of the signals.

a. $\overline{EA}$ b. RXD

(5+3+2)

3A. With neat diagram, explain the 8051 port 1 pin structure. With the help of this structure, explain why logic-1 should be sent to the port to make it as input port.

3B. Write and explain the IVT and IE register format of 8051. Write the interrupt priority order immediately after reset.

3C. Instruction, ***JZ FEH,*** is stored at **9490H**. What is the PC value if the condition is true and if it's false?

(5+3+2)

4A. Two switches SW0 and SW1 are interfaced to 8051 using ***PORT-2.*** Write a program to send *00H* to ***PORT-0*** when key SW0 is pressed. If key SW1 is pressed, send *FFH* to ***PORT-1***. Poll the keys continuously.

4B. Write all the affected register contents after LDR r0, [r1, #4]! instruction gets executed if the initial contents of the registers are as given below. r0 = 0x00000000, r1 = 0x00090000, mem32 [0x00009000] = 0x01010101, mem32 [0x00009004] = 0x02020202.

Assuming the given initial conditions in the first case, write the register contents after the execution of LDR r0, [r1], #4 instruction.

4C. Write the multiple register transfer instruction pair, for performing PUSH and POP operations in the case of ED type of stack.

(5+3+2)

5A. Describe with a neat diagram, the data flow model of ARM core.

5B. With an example for each, explain following ARM assembler directives:

i. ENTRY ii. EQU iii. SPACE

5C. With interface circuit develop an assembly language program to blink the LED connected to P0.5 of 8051 continuously at a frequency of 20 Hz. Use timer-0 in mode-1.

(5+3+2)