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# MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
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**FIFTH SEMESTER B.Tech (E & C) DEGREE END SEMESTER EXAMINATION**
**NOV/DEC 2017**
**SUBJECT: VLSI DESIGN (ECE -3104)**

**TIME: 3 HOURS** **MAX. MARKS: 50**

**Instructions to candidates**
- Answer **ALL** questions.
- Missing data may be suitably assumed.
- Grid Sheet/ graph sheet will be provided.

1A. An enhancement type NMOS transistor with $V_t$ = 0.7V has its source terminal grounded and a 1.5-V DC is applied to the gate. In what region does the device operate: for (i) $V_D$ = +0.5 V (ii) $V_D$ = +0.9 V (iii) $V_D$ = +3 V.

In the NMOS device, $\mu_n C_{ox}$ = 100 µA/V$^2$ , W = 10 µm, and L = 1 µm, find the value of drain current that results in each of the three cases (i), (ii), and (iii).

1B. Apply Constant Voltage scaling model to (i) switching energy per gate (ii) Current density (iii) Saturation current.

1C. Draw the stick diagram of CMOS circuit shown in figure 1C.

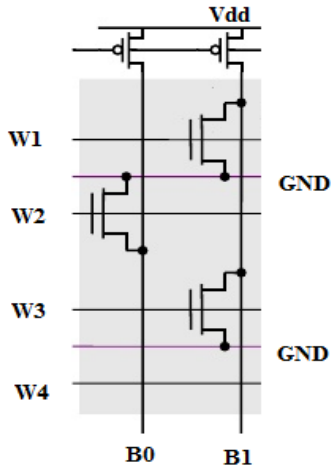



**Figure 1C.**

(5+3+2)

2A. Draw the layout of CMOS based circuit with F= NOR (a, b) with pull-down ratio fixed to ½.

2B. Derive the Zpu/Zpd ratio of pseudo NMOS inverter driven by similar inverter.

2C. Draw the voltage transfer characteristic (VTC) curve for (i) Resistive load based and (ii) Enhancement pull up based NMOS inverter.

(5+3+2)

3A. Explain the fabrication of NMOS enhancement mode transistor with neat diagram.

3B. Consider the multilayer structure shown in **FIG. 3B**. Given that λ = 2.5 μm. Refer the **Table I** for area capacitance calculation.

(i) A 3λ wide metal path crosses a 2λ wide polysilicon path at right angles. The layers are separated by a 0.5 μm thick layer of silicon dioxide. Find the capacitances associated with metal layer.

The polysilicon layer in turn crosses a 4λ wide diffusion region at right angles to form a transistor. Find the capacitance associated with poly layer.

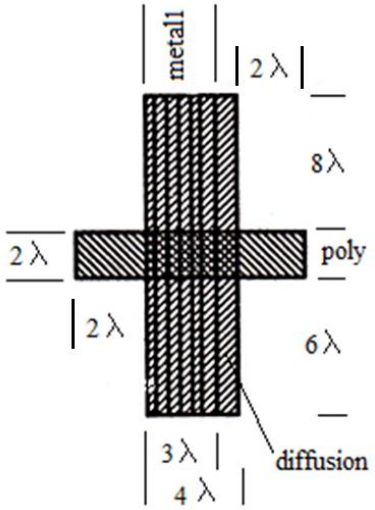



**Figure 3B.**

**Table I Typical values of area capacitance for 5 μm technology**

| *Capacitance* | *Value in pF × $10^{-4}$/μm²* *(Relative values in brackets)* | |
|---|---|---|
| Gate to channel | 4 | (1.0) |
| Diffusion (active) | 1 | (0.25) |
| Polysilicon* to substrate | 0.4 | (0.1) |
| Metal 1 to substrate | 0.3 | (0.075) |
| Metal 2 to substrate | 0.2 | (0.05) |
| Metal 2 to metal 1 | 0.4 | (0.1) |
| Metal 2 to polysilicon | 0.3 | (0.075) |

3C. Explain the effect of change in power supply on voltage transfer characteristic (VTC) of the CMOS inverter.

(5+3+2)

4A. Explain the working of ALU using adder as an element. Perform following operation using ALU

(i) 1101+0101 (ii) 1101 EXOR 0101 (iii) stick diagram of adder (NMOS based).

4B. Give the implementation of output $Z = V_1.A + V_2.B + V_3.\bar{C} + V_4.D + V_5.E$ using suitable switch based logic such that there is no degradation of output voltage level. Given that $V_1$, $V_2$, $V_3$, $V_4$ and $V_5$ are data inputs and the control inputs A, B, $\bar{C}$, D and E are mutually exclusive. Draw the stick of

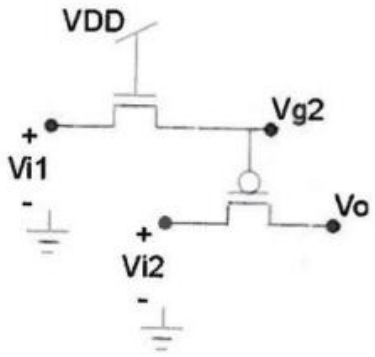
same.

4C. Implement 2x2 cross bar switch to show (i) 1-bit left (ii) no shift operation.

(5+3+2)

5A. Explain with neat circuit/diagram the following (i) Electromigration (ii) Tristate buffer design for Bus.

5B. Find Vg2 and Vo in the two-transistor circuit shown in Figure 5C for each of the listed input voltage combinations. Assume VDD = 3V, Vtn = 0.5V, and |Vtp| = 0.4V.




(i) Vi1=0.2 V,Vi2=3 V (ii) Vi1=1 V,Vi2=2 V (iii) Vi1=1.5 V,Vi2=1 V

5C. Give the implementation of 3-bit Johnson counter using 1-bit shift register stages (NMOS) with two phase non-overlapping clock. The shift register stages have built-in parallel load feature.

(5+3+2)