Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

FIFTH SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION
NOV 2017
SUBJECT: VLSI DESIGN (ECE -3104)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.
- Grid or graph sheet can be used for Layout..

1A. Explain the WR and RD operation of 3T- DRAM cell. Draw the stick of one cell.

1B. In a CMOS inverter given that V_{thn} = 0.83 V, V_{thp} = - 0.8 V, V_{dd} = 3 V. Find the value of gate threshold V_{inv} for following cases : [i] $\beta_n = 0.4\beta_p$ [ii] $\beta_n = 2.5\beta_p$.

1C. Can we replace the circuit shown in Figure 1B with a single MOSFET? If yes, give the necessary length and width of equivalent MOSFET. Also, give an expression for the transconductance. Note: both the MOSFET transistors are identical.

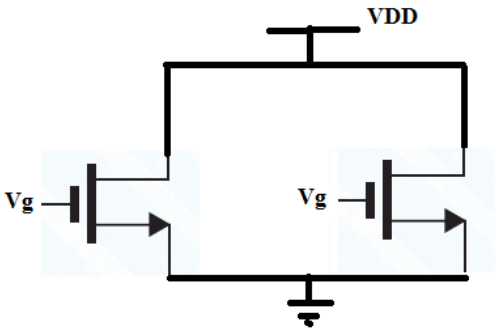

Figure 1B.

(5+3+2)

2A. Implement a 2-bit binary up counter using NMOS switch logic and 1- bit dynamic memory element.

2B. Given Kn=100 µA/V^2, λ=γ=0. Vs=Vb=2 V . Vd=3V, V_{THO} = 0.5 V. The current into terminal D shown in Figure 2B is 2mA. What is Vg ?

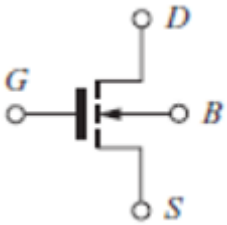

Figure 2B.

2C. Two inverters (CMOS) are cascaded to drive capacitive load, C_L=15 C_g as shown in Figure 2C. Calculate the delay of each stage. R_{sn}=10kΩ and Cg (2µm) = 0.005 pF. Consider both inputs '1' and '0'. V_{dd} = 3V, R_{sp} = 3R_{sn}.

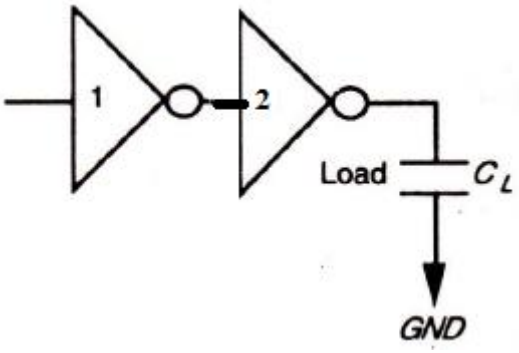

Figure 2C.

Sl.No	INV1	INV2
Pull-up	L=8λ,W=2 λ	L=2λ,W=6 λ
Pull-down	L=2λ,W=2 λ	L=2λ,W=2 λ

(5+3+2)

3A. Draw the CMOS layout of 2-input NAND gate for asymmetrical switching time.

3B. Implement following words: word1: 1011, word2: 0110, word3: 1010, w4:1111 using pseudo NMOS NOR ROM. Draw the stick of the same.

3C. Draw the cross-section and circuit diagram of a CMOS inverter assuming:
i. Twin-tub process;
ii. N-well process;
Label all relevant regions (n-well, p-well, n+, p+, metal1, poly) and draw connections to V_{dd} and Gnd. Show transistors as 4-terminal devices.

(5+3+2)

4A. Implement following functions (i) $Y = \overline{AB + C}$ (ii) $Y = \overline{(A \odot B)}$ (iii) Y= AB using Dynamic CMOS based PLA with stick diagram.

4B. Mention 3 important advantages of SOI process over bulk CMOS.

4C. (i) Define Regularity. (ii) Standard cell used to implement a Four-line Gray Code to Binary Code Converter is …….

(5+3+2)

5A. Today's technology demand IC packages of 1000 pins. The simultaneous switching of a lot pads, each driving a large capacitor, causes large transient currents and creates voltage fluctuations. In order to overcome these, Engineer's from INTEL have come to design an output stages of buffer. The design is as follows`

The IC's (NMOS based) on-chip minimum size inverter has to drive an off-chip capacitor C_L = 20 pF in 1.2 um technology (Cg=0.0023 pF). What will be the Engineer's calculation for

(i) Requirement of Number of stages (ii) Total delay (iii) Ratio of each stages.

5B. Apply constant electric field scaling to (i) switching energy (ii) Current density (iii) Saturation current.

5C. Draw the stick Notation of a sense amplifier used in SRAM cell.

(5+3+2)