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MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

VII SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, NOVEMBER 2017

SUBJECT: EMBEDDED PROCESSOR ARCHITECTURE [ELE 4003]

REVISED CREDIT SYSTEM

Time: 3 Hours **Date: 23 November 2017** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. Discuss the embedded platform characteristics in detail. ***(05)***

1B. Write the PC behaviour in 3-stage and 5-stage pipeline organization. ***(03)***

1C. The NRE cost and time to prototype involved in designing an ES is $500 and 1 month respectively. The unit cost involved in designing a single unit is $100 and the design turn-around time is 2months. Total 100 units are produced. Calculate the total cost and the time to market. ***(02)***

2A. Draw and explain the MU0 register transfer level (RTL) organization. With reference to RTL diagram write the control logic for the following instructions and explain.

STO S, SUB S, JNE S, STP ***(05)***

2B. Explain with the instruction format, Thumb mode entry and exit. ***(03)***

2C. Give the functions performed by a basic ARM memory control logic. ***(02)***

3A. What is boundary scan? Explain the ARM debug system. Write the advantages of using JTAG port in the debug architecture. ***(05)***

3B. Write the branch and branch with link instruction format. With the diagram explain the data path activity for branch with link instruction in a 3 stage pipeline organization. ***(03)***

3C. Consider an ARM 3 stage pipeline, illustrate the pipeline operation with the help of a diagram for the sequence of code given below. Write the number of clock cycles required for the execution. What is the content of PC when "ADD" instruction is under execution? What is the content of r14 when "BL" instruction is under execution?

```
0x00000000  start: MOV r1,r2
0x00000004         CMP r1,r5
0x00000008         ADD r2,r5
0x0000000C         BL loop1
0x00000010         SUB r5,r7
0x00000014         END
0x00001000  loop1: ADDC r1, r3
0x00001004         MOV pc, r14.
```

(02)

4A. Draw a typical finite state machine for task execution states. Three processes with process IDs P1, P2, P3 with estimated completion time x, y, z milliseconds respectively enters the ready queue. The average TAT is 13ms and average waiting time is 5.66ms. The waiting time and execution time for process P3 is 5ms and 7ms respectively. The waiting time for process P2 is 0ms. TAT for P1 is 22ms. Assume there is no I/O waiting for the processes and all the processes contain only CPU operation and no I/O operations are involved. Complete the table shown below and also determine the scheduling algorithm adopted. Justify the answer.

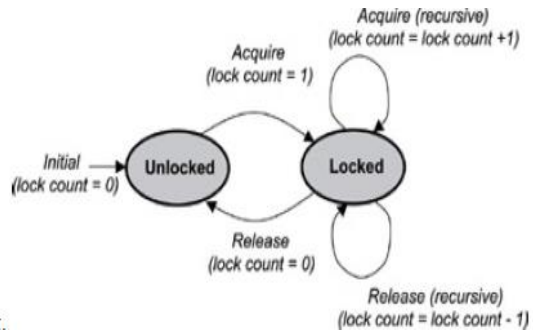
process	execution time	waiting time
P1	x	a
P2	y	b
P3	z	c

(05)

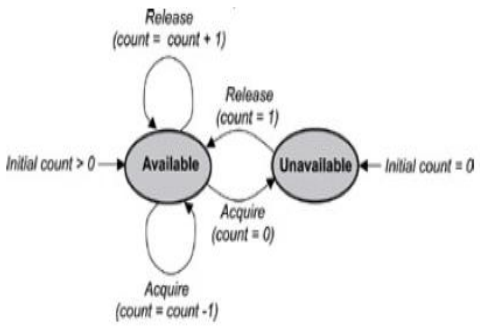
4B. Discuss the efficient implementation of FIR filters on the ARM with relevant equations. ***(03)***

4C. Identify the state diagrams of the following kernel objects and define them.

i)



ii)



(02)

5A. Give the objectives of AMBA specification. Draw the typical AMBA based system. Define the various AHB-Lite signals. Draw the timing diagram for read transfer and write transfer in AHB with one wait state. ***(05)***

5B. What is bit banding in ARM cortex processor? Analyse bit banding with the traditional method of bit access. ***(03)***

5C. List any four features of .ARM cortexM3 processor which delivers high performance in microcontroller products. ***(02)***