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MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent Institution of MAHE, Manipal)

VII SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

MAKE-UP EXAMINATIONS, DECEMBER 2017

FPGA BASED SYSTEM DESIGN [ELE 4002]

REVISED CREDIT SYSTEM

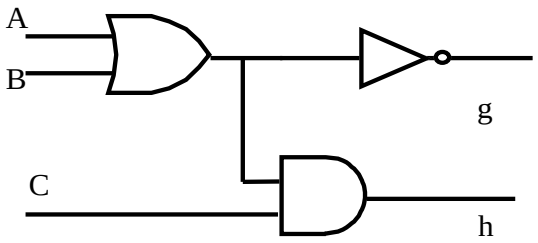
Time: 3 Hours **Date: 30 December 2017** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. With neat flowchart, list the steps involved in FPGA design flow. ***(03)***

1B. Develop the test vectors to test the logic circuit below for all stuck at faults.



(03)

1C. Implement full subtractor using Actel ACT-1 module. How many numbers of modules are used? ***(04)***

2A. Explain the structure of CLB in Xilinx SPARTAN - IIE FPGA highlighting its usage. ***(04)***

2B. Suggest a programming technology suitable for the following specifications and explain it in detail. i) Device cannot be reconfigured in circuit ii) Configuration is non-volatile ***(03)***

2C. Implement a 4 to 1 mux using PLA by considering appropriate size for the inputs and gate planes ***(03)***

3A. What are the important features and advantages of dynamically reconfigurable FPGAs? ***(04)***

3B. Design an encoder for use in a domestic burglar alarm that has sensors for each of eight zones. Each sensor signal is 1 when an intrusion is detected in that zone, and 0 otherwise. The encoder has three bits of output, encoding the zones. Develop a Verilog model of an encoder for the code used in the burglar alarm. ***(03)***

3C. Develop a Verilog test-bench model for 2:4 decoder (Verilog model for 2:4 decoder is not necessary). ***(03)***

4A. Draw the state diagram of logic design shown in Fig 4A.

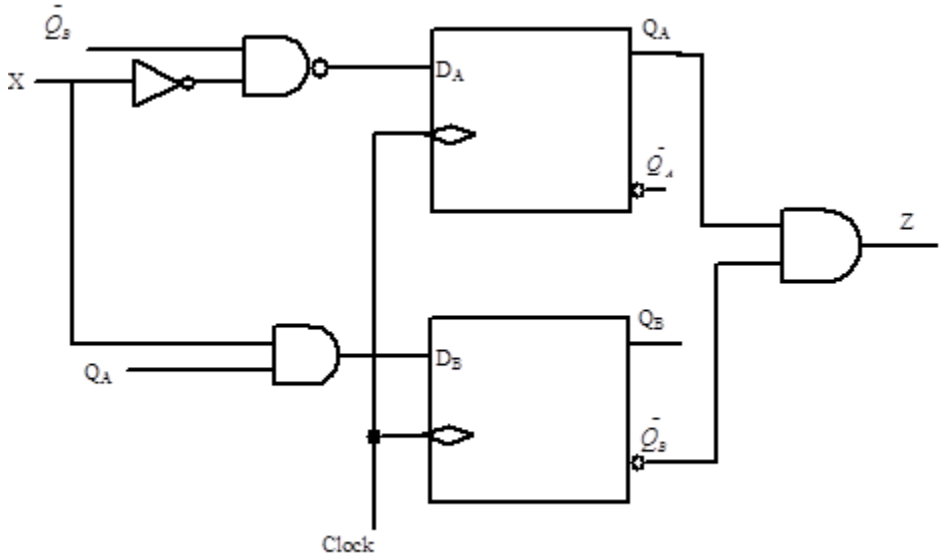


Fig. 4A ***(04)***

4B. An 8:1 multiplexer with an active high enable is to be implemented using Xilinx SPARTAN-II E FPGA. Draw its circuit schematic specifying the contents of the LUTs. How many CLBs are needed for the implementation? ***(04)***

4C. Write a note on BIST. ***(02)***

5A. Find the distinguishing sequence for the following state table and find the inputs to verify all the transitions.

State	Next state		Output	
	X=0	X= 1	X=0	X=1
S0	S0	S1	0	0
S1	S0	S2	1	1
S2	S3	S3	1	1
S3	S2	S0	1	0

(04)

5B. What are the advantages and disadvantages of FPGA based implementation option compared to ASIC based implementation? ***(02)***

5C. Design a digital system that multiplies two 4 bit numbers using full adder and AND gates. Explain the algorithm used with an example. ***(04)***