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MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

VII SEMESTER B.TECH (ELECTRICAL & ELECTRONICS ENGINEERING)

END SEMESTER EXAMINATIONS, NOVEMBER 2017

SUBJECT: FPGA BASED SYSTEM DESIGN [ELE 4002]

REVISED CREDIT SYSTEM

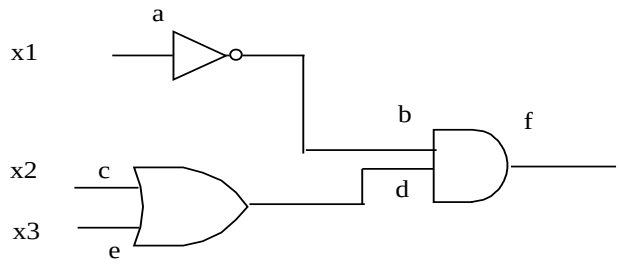
Time: 3 Hours **Date: 25 November 2017** **Max. Marks: 50**

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A. How PALs are different from PLAs? Draw the logic circuit which gives additional flexibility to PAL. ***(03)***

1B. Develop the test vectors to test the logic circuit below for all stuck at faults.



(03)

1C. Implement full adder using Actel ACT-1 module. How many numbers of modules are used? ***(04)***

2A. Sketch and explain the functional block diagram of Xilinx SPARTAN - IIE FPGA. ***(04)***

2B. Suggest a programming technology suitable for the following specifications and explain it in detail. i) Device can be reconfigured in circuit ii) Configuration is volatile iii) Allows fast reconfiguration ***(03)***

2C. With the help of circuit diagram explain a typical boundary scan cell. ***(03)***

3A. Differentiate between reconfigurable logic and dynamically reconfigurable logic. What are the important features of dynamically reconfigurable FPGAs? Which programming technologies are used in dynamically reconfigurable FPGAs? ***(04)***

3B. Suppose a factory has two vats, only one of which is used at a time. The liquid in the vat in use needs to be at the right temperature, between 25˚C and 30˚C. Each vat has two temperature sensors indicating whether the temperature is above 25˚C and above 30˚C, respectively. The vats also have low-level sensors. The supervisor needs to be woken up by a buzzer when the temperature is too high or too low or the vat level is too low. He has a switch to select which vat is in use. Develop a Verilog model that expresses the logical structure to activate the buzzer as required. Assume that the sensor signals and the switch signal are inputs to the model, and that the buzzer signal is the output from the model. ***(03)***

3C. Develop a Verilog test-bench model for 2:1 multiplexer (Verilog model for 2:1 multiplexer is not necessary). ***(03)***

4A. Draw the synthesized circuit for the Verilog code (Multiplication function) given below. How many clock cycles are required to complete the multiplication?

```
module mult8( output done, output reg [7:0] product, input [7:0] A, input [7:0] B, input clk,
input start);
reg [4:0] multcounter; // counter for number of shift/adds
reg [7:0] shiftB; // shift register for B
reg [7:0] shiftA; // shift register for A
wire adden; // enable addition
assign adden = shiftB[7] & !done;
assign done = multcounter[3];
always @(posedge clk) begin // increment multiply counter for shift/add ops
if(start) multcounter <= 0;
else if(!done) multcounter <= multcounter + 1; // shift register for B
if(start) shiftB <= B; else shiftB[7:0] <= {shiftB[6:0], 1'b0}; // shift register for A
if(start) shiftA <= A;
else shiftA[7:0] <= {shiftA[7], shiftA[7:1]}; // calculate multiplication
if(start) product <= 0;
else if(adden) product <= product + shiftA;
end
endmodule
```

(04)

4B. Realize five bit prime number detector using Spartan IIE FPGA. How many CLBs are required for the implementation ***(04)***

4C. Draw a schematic diagram for an LFSR (pseudo-random number generator) with n=4 that generates a maximum length sequence. Mention the generated random number sequence. ***(02)***

5A. Find the distinguishing input sequence for the following state table to verify all the state transitions. Prove the same.

PS	NS (x=0)	NS (x=1)	o/p (x=0)	o/p (x=1)
S0	S2	S3	1	0
S1	S3	S1	0	1
S2	S1	S2	0	1
S3	S2	S0	0	0

(04)

5B. What are the benefits of using a soft embedded processor in an FPGA over a hard macro implementation? ***(02)***

5C. Implement divider circuit using basic full adder/subtractor cell. Explain the logic with an example. ***(04)***