Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

SEVENTH SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION
NOV/DEC 2017
SUBJECT: ANALOG MIXED SIGNAL DESIGN (ECE - 4013)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. With neat diagram explain Noise shaping oversampling ADC and how Oversampled ADCs allow signal bandwidth to be efficiently traded for resolution.

1B. Design a 3 bit charge scaling Digital to Analog Converter and find the value of the output voltage for $D_2D_1D_0$= 010 and 101. Assume that V_{ref}=5V and C=0.5pF.

1C. What is the equivalent resistance of a 5pF capacitor sampled at a clock frequency of 100 kHz.

(5+3+2)

2A. With neat diagram and example explain the need for specialized CMOS technology characterization for analog design.

2B. Realize following using OTA building blocks: i) Negative resistor ii) Floating Inductor

2C. What are the issues related to mixed signal design? Explain strategies used to resolve the problem.

(5+3+2)

3A. Design the KHN OTA-C biquad for realizing band pass filter for Q=5, f_c= 1MHz. Assume $C_1 = C_2$ = 10 pF.

3B. Explain passive and active compensation methods for compensation of finite bandwidth effects.

3C. What are the advantages of current mode over voltage mode filter structures

(5+3+2)

4A. Consider the triple cascode current sink. Assume all transistors operating in saturation region with Id=10µA, V_{ds}=5V, $g_m r_0$=50. Find the value of output impedance. Neglect the bulk effect.

4B. Consider the differential input single ended output NMOS gain stage using PMOS current mirror as active load. Given that i_{bias}=200µA and all transistors have W/L = 100µm/1.6µm, $\mu_n C_{ox}$ = 92µA/V^2, V_{thn} = 0.8V, early voltage $V_{En,p}$ = 8V/m. Find the output impedance in differential amplifier stage and the differential gain.

4C. What are the merits and demerits of cascode connection in current mirror circuit?

(5+3+2)

5A. Consider a NMOS based common source amplifier with a current mirror active load where in all the transistors have W/L =100µm/1.6µm. Given that $\mu_n C_{ox}$ = 90µA/V^2, I_{bias} = 100µA, λn = 0.078125/V and λp = 0.082/V.

5B. Find the resolution for a Digital to Analog Converter, if the output voltage is desired to change in 1 mV increments while using a reference voltage of 5V.

5C. Why balanced filter structures are preferred in industry over single ended filter structures?

(5+3+2)