Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

SEVENTH SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION
NOV 2017
SUBJECT: ANALOG MIXED SIGNAL DESIGN (ECE - 4013)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. With a neat diagram explain mixed signal layout strategy used to improve the performance of analog circuitry.

1B. Design a current sink using V_{DD}=-V_{SS}=2.5V to sink a current of 10µA.Estimate the minimum voltage across the current sink and the output resistance. Using the 10µA n-channel current sink, design 3 current sources with the value of 10µA, 20µA and 50µA, V_{gs}=1.2V, K_n=50µA/V^2 ,K_p=17µA/V^2,L=5µm.

1C. Explain the term sensitivity with respect to current mirror. Estimate the variation in I_0 ,for the above current mirror for V_{DD} changing from 2.4V to 2.6V.

(5+3+2)

2A. With neat diagram of analog design octagon, explain trade-offs and challenges present in the design of high performance amplifiers.

2B. Design a Tow-Thomas bi-quad for realizing band pass filter for Q=5, f_c= 1MHz. Assume C_1=C_2=10pf and g=62.83µS.

2C. Explain advantages of current-mode signal processing as compared to voltage-mode signal processing

(5+3+2)

3A. Consider the current mirror with source degeneration in which Iin=100µA.Each transistor has W/L =100µm/1.6µm, R_s=5kΩ. Given that $\mu_n C_{ox}$ = 92µA/V^2 , V_{thn} = 0.8V,R_{ds}=128kΩ. Find the output resistance of the current mirror .Assume the body effect can be approximated by gmb_2=0.2gm

3B. Design 4th order 455kHz unity gain Butterworth LPF with normalized transfer function given by:

$$\frac{1}{s^4 + 2.613s^3 + 3.414s^2 + 2.613s + 1}$$

3C. Using switched capacitor technique implement the passive RC first order LPF, so that product of RC is 1msec and 3dB frequency is 159Hz.

(5+3+2)

4A. A PMOS active loaded MOS differential amplifier has the following specifications: L=5µm, $(W/L)_n$=100, $(W/L)_p$=200 , $\mu_n C_{ox}=2\mu_p C_{ox}$= 0.2 mA/$V^2$, $I_{SS}=I_{bias}$=0.8mA, R_{SS}=25kΩ,$V_{En,p}$= 4V/µm. Find i) R_0 ii) A_d iii) A_{cm} iv)CMRR

4B. With neat block diagram explain the difference between nyquist rate and oversampling ADC's. What are the advantages of oversampled converters.?

4C. What are the advantages of fully differential style employed in Analog and Mixed signal circuit design?

(5+3+2)

5A. Sketch and explain the block diagram of a first-order sigma-delta modulator. Use a time discrete integrator with the transfer function $H(z) = \frac{1}{z-1}$.

5B. Design 6 bit charge scaling DAC using a split array and find the value of the output voltage for i) $D_5D_4D_3D_2D_1D_0$=100000, ii) $D_5D_4D_3D_2D_1D_0$=000001. Assume V_{ref}=5V and C=0.5pF

5C. With neat diagram explain phase compensated gm active RC lossy integrator.

(5+3+2)