Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

SEVENTH SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION
NOV/DEC 2017
SUBJECT: LOW POWER VLSI DESIGN (ECE - 4014)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates

- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Explain Power supply gating technique with the design issues for leakage power reduction using suitable circuits. What are its merits and demerits?

1B. Discuss various clock gating and pre computation schemes for low power operation.

(5+5)

2A. Describe dual V_{dd} technique with its salient features for reducing dynamic power in CMOS circuits.

2B. Explain implementation of low swing busses for power reduction in VLSI circuits highlighting it's merits and demerits.

(5+5)

3A. Explain i) bus segmentation technique and ii) Bus encoding techniques for reducing bus power in VLSI circuits.

3B. With the help of suitable illustration show FSM encoding for reducing dynamic power dissipation.

(5+5)

4A. Discuss various sources of leakage in MOSFETs and suggest two techniques each for reducing leakage current.

4B. Discuss the impact of crosstalk and techniques employed to reduce crosstalk in interconnects.

(5+5)

5A. Discuss Dynamic Power Management Policies and compare them.

5B. With suitable examples explain i) Procrastination scheduling and ii) Loop unrolling technique for low power designs.

(5+5)