Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

SEVENTH SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION
NOV 2017
SUBJECT: LOW POWER VLSI DESIGN (ECE - 4014)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Discuss the motivation for low power VLSI and basic strategies to reduce power dissipation in VLSI.

1B. Starting from fundamentals derive the expression for switching power in CMOS circuit and explain the significance of the expression from the low power point of view.

(5+5)

2A. Illustrate with examples the following techniques: i) Input ordering ii) Logic restructuring and iii) guarded evaluation

2B. Discuss i) Role of low swing bus in VLSI with its salient features and ii) FSM encoding with suitable illustration.

(5+5)

3A. Discuss i) Repeaters in interconnects and its impact ii) Techniques to reduce cross talk.

3B. Certain chip in 90nm CMOS process consists of 400 million transistors of width 0.18µm and works on 1.2 Volts supply. If the OFF transistors experience a current of 20nA/µm and 5nA/µm for Low and High V_{th} respectively, calculate the leakage power if i) All the transistors are of low V_{th} ii) 30% of the transistors are of low V_{th} and rest of them are high V_{th}. What is the percentage saving in power? iii) Describe the low power technique used in the above example.

(5+5)

4A. List the main sources of leakage power dissipation n in deep sub-micron devices and discuss at least one remedy for each of them.

4B. Explain two methods each for i) Design time technique and ii) run time technique for reducing leakage power.

(5+5)

5A. Discuss the memory optimisation techniques for reducing the system level power reduction.

5B. Explain with the help of suitable expressions the basic principle of adiabatic switching and discuss the challenges involved in its implementation.

5C. Assume that the HDD in your lap top has an average transition delay (shut down and wake up) of 50 ms, power in sleeping and working state are 10mW and 100 mW respectively. Also, the transition energy is of 50 mW-sec. Calculate the minimum idle time required to consider switching to power down mode.

(5+3+2)