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# MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

*A Constituent Institution of Manipal University*

**SEVENTH SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION**
**NOV 2017**
**SUBJECT: LOW POWER VLSI DESIGN (ECE - 429)**

**TIME: 3 HOURS** **MAX. MARKS: 50**

**Instructions to candidates**

- Answer any **FIVE FULL** questions.
- Missing data may be suitably assumed.

1A. Explain the need for low power design and discuss hierarchy of low power design strategies.

1B. What are the components of power dissipation in CMOS? Explain. Starting from the fundamentals derive the expression for switching power in a CMOS inverter and indicate how we can reduce switching power.

(5+5)

2A. Explain the use of Dual supply voltage in VLSI circuits to reduce dynamic power. List the drawbacks of the technique and suggest remedies.

2B. Discuss architectural level power reduction techniques and compare them.

(5+5)

3A. Discus i) T0 coding and ii) Bus invert coding. Also give your comments on their applicability.

3B. Illustrate the use of repeaters in interconnects and their impact on power and delay.

(5+5)

4A. What are the main sources of leakage power dissipation in MOS transistor? List and explain.

4B. With the help of simple illustration, explain dual Vth technique for leakage reduction in VLSI circuits.

(5+5)

5A. Describe the device level techniques for leakage power reduction.

5B. Mention any three techniques employed in coding / software to effect power reduction. Explain each of them.

(5+5)

6A. Discuss memory optimisation technique for system level power reduction.

6B. List and explain the DPM policies with their salient features.

(5+5)

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