Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY
MANIPAL
A Constituent Institution of Manipal University

SEVENTH SEMESTER B.Tech. (E & C) DEGREE END SEMESTER EXAMINATION
NOV 2017
SUBJECT: RTL VERIFICATION USING VERILOG (ECE - 4021)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Apply LIST-L Scheduling algorithm for the given data flow graph shown in Fig.Q1A. Assume γ=4, $M_1=M_2=M_3=M_4=M_5=0$; $M_6=M_7=1$; $M_8=M_9=M_{10}=M_{11}=2$. Draw the scheduled graph under resource constraints.

1B. Draw the Control and data flow graph(CDFG) for the statements A=B*C+D, while A>0, then A=A-1 else end loop.

1C. Explain about the steps of high level synthesis.

(5+3+2)

2A. Find the essential prime implicant for the set of prime implicants F={C_1, C_2, C_3, C_4} where $C_1=x_1'x_3'x_4'$, $C_2=x_1x_2$, $C_3=x_3x_4$, $C_4=x_2x_3'x_4'$ using ESPRESSO algorithm.

2B. Explain force directed scheduling algorithm with an example.

2C. Write the Verilog AMS code for the given expression to calculate i= C.dv/dt. The values can be suitably assumed.

(5+3+2)

3A. Construct an ROBDD for a 2 bit synchronous up counter. Also Apply ITE algorithm for the same.

3B. Consider the following state table, Minimize the states using Implication chart. Draw the reduced state diagram.

Present State	Next State When x=0	Next state When X=1	Output (Z) When x=0	Output(Z) When x=1
A	A	B	0	0
B	D	C	0	1
C	F	E	0	0
D	D	F	0	0
E	B	G	0	0
F	G	G	0	1
G	A	F	0	0

3C. Explain heuristic minimization. What are all the different types of heuristic minimizers available.

(5+3+2)

4A. Write the Verilog analog mixed signal (V_{ams}) code for the circuit shown in Fig. Q4A.

4B. Determine the prime implicants for the following function using iterated consensus method F=x'z'+xyz'+xy'z'+xy'z.

4C. Explain Gajski' Y chart.

(5+3+2)

5A. Consider the scheduled graph for the given unscheduled dataflow graph shown in Fig:1 Apply clique partitioning algorithm and determine the operation binding resources for MUL and ALU. Show all the steps(comparability graph, conflict graph and operation binding solution).

5B. Determine the complement of the following function using Shannon's expansion theorem F=wx'y+w'xy+yz'+wxy'+wy'z'.

5C. Explain the process of Model checking verification technique.

(5+3+2)

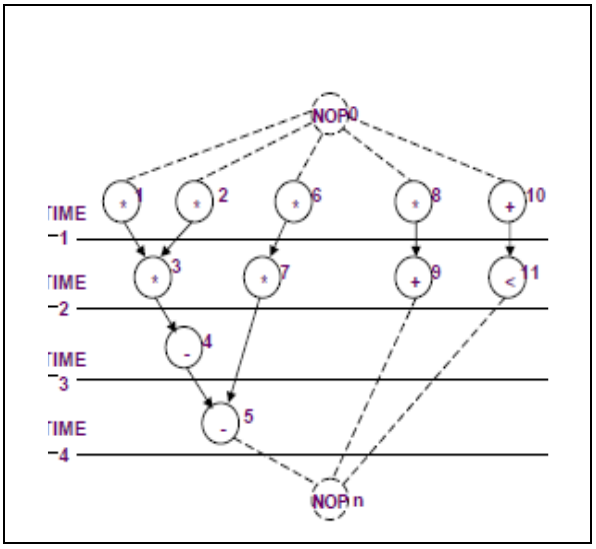

Fig: Q1A

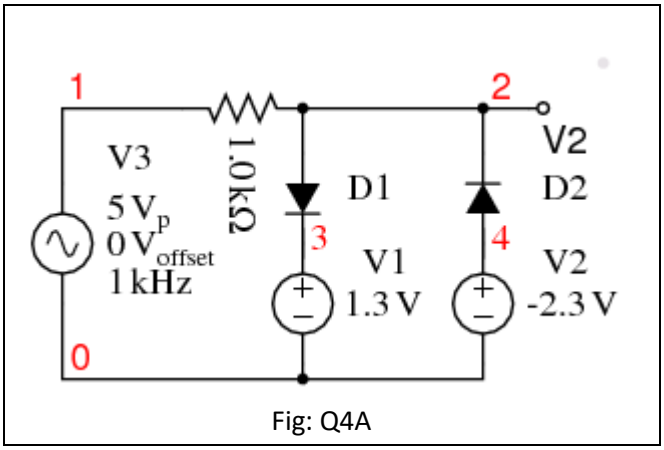

Fig: Q4A