Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

SEVENTH SEMESTER B.TECH. (INSTRUMENTATION AND CONTROL ENGG.)

END SEMESTER EXAMINATIONS, DEC - 2017

SUBJECT: VLSI DESIGN [ICE 4004]

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Missing data may be suitably assumed.

1A Illustrate the pMOS fabrication process with diagrams. 4

1B Obtain the expression for the drain to source current in the saturated region of a MOSFET. 3

1C Briefly explain the importance of MOS transistor threshold voltage. What are the factors affecting it? Illustrate with equations. 3

2A Compare the various CMOS fabrication techniques by listing the advantages and disadvantages of each of them. 4

2B Find the ratio $\frac{\beta_n}{\beta_p}$ needed to obtain an inverter midpoint voltage of V_M=1.3 V with a power supply of 3 V. Assume that V_{Tn}=0.6 V and V_{Tp}=-0.82 V. What would be the relative device sizes if K_n=110 μA/V^2 and the mobility values are related by μ_n=2.2μ_p? 3

2C Sketch a transistor-level schematic and stick diagram/layout of a 2-input NAND gate. 3

3A Draw the equivalent RC circuit of a 3-input NAND gate. 3

3B Sketch a transistor-level schematic of a SR flip-flop. 3

3C Illustrate the generalized flow of standard cell place and route with a flowchart. 4

4A Explain the structured design techniques. 3

4B Briefly explain the various programming technics used in FPGA. 4

4C Find a minimum-row PLA table to implement the following equations: 3

$$x(A,B,C,D) = \sum m(0,1,4,5,6,7,8,9,11,12,14,15)$$

$$y(A,B,C,D) = \sum m(0,1,4,5,8,10,11,12,14,15)$$

$$z(A,B,C,D) = \sum m(0,1,3,4,5,7,9,11,15)$$

5A Implement a 4:1 MUX using an MUX based FPGA configurable logic block. 3

5B Compare each of the following four ASIC subcategories: 4

(a) PLDs

(b) Gate Arrays

(c) Standard-cell

(d) Full-custom

5C Explain the general structure of a scan-based design with figure. 3