Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

A Constituent Institution of Manipal University

SEVENTH SEMESTER B.TECH. (INSTRUMENTATION AND CONTROL ENGG.)

END SEMESTER EXAMINATIONS, NOV - 2017

SUBJECT: VLSI DESIGN [ICE 4004]

Time: 3 Hours MAX. MARKS: 50

Instructions to Candidates:

- Answer **ALL** the questions.
- Use neat diagrams where ever needed.

1A Illustrate the nMOS fabrication process with diagrams. 4

1B Obtain the expression for drain to source current in non-saturated region of a MOSFET. 3

1C Determine the pull-up to pull-down ratio for an nMOS inverter driven by another nMOS inverter. 3

2A An inverter uses FETs with β_n=2.1 mA/V^2 and β_p=1.8 mA/V^2. The threshold voltages are given as V_{tn}=0.6 V and V_{tp}=-0.7 V and the power supply has a value of V_{DD}=5 V. The parasitic FET capacitance at the output node is estimated to be C_{FET}=74 fF.

1. Find the midpoint voltage V_M.
2. Find the values of R_n and R_p.
3. Calculate the rise and fall times at the output when C_L=0.
4. Calculate the rise and fall times when an external load of value C_L=115 fF is connected to the output. 4

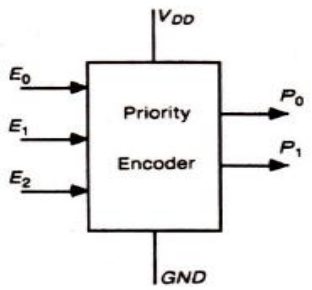
2B Sketch a transistor-level schematic and stick diagram/layout for the following function:

$$Y = \overline{AB + C.(A + B)}$$ 4

2C What is body effect? How does it affect the operation of a MOSFET? 2

3A Draw the equivalent RC circuit of a 2-input XOR gate. 3

3B Construct a color-coded stick diagram to implement a priority encoder as in the following table:



E_2	E_1	E_0	P_1	P_0
0	0	0	0	0
0	0	1	1	1
0	1	0	1	0
0	1	1	1	0
1	0	0	0	1
1	0	1	0	1
1	1	0	0	1
1	1	1	0	1

4

3C Sketch a transistor-level schematic of a JK flip-flop. 3

4A Illustrate the design flow of a mixed-signal system with a flowchart. 4

4B Briefly explain the types of basic logic cells employed in a programmable ASIC. 3

4C Implement the following state table using a ROM and two D flip-flops:

Present State	Next State $X = 0$	Next State $X = 1$	Output (Z) $X = 0$	Output (Z) $X = 1$
S_0	S_0	S_1	0	1
S_1	S_2	S_3	1	0
S_2	S_1	S_3	1	0
S_3	S_3	S_2	0	1

3

5A Implement a 4:1 MUX using a 4-input LUT based FPGA configurable logic block. 3

5B Briefly explain the different fault types and models. 3

5C What are the essential circuit models required for Built-in-self-test (BIST)? Illustrate them with figures. 4

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