Question Paper

Exam Date & Time: 27-Apr-2018 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES
SECOND B.Sc (APPLIED SCIENCES)
END-SEMESTER THEORY EXAMINATIONS APRIL - 2018
DATE : 27 APRIL 2018
TIME : 9:30AM TO 12:30PM

Computer Organization and Architecture [ICS 122]

Marks: 100 **Duration: 180 mins.**

Answer 5 out of 8 questions.

Missing data, if any, may be suitably assumed

1)		Draw the block diagram showing the interconnections between processor and memory and explain the various components in it. Also explain the typical operating steps in a computer system.	(8)
	A)		
	B)	Convert the following pair of decimal numbers to 5-bit 2's-complement numbers, then perform addition and subtraction on the pair. -12 and 3	(4)

	C)	Identify the addressing mode of the source operand(s) in each of the following instructions and explain the same.
		Load R2, (R5)
		Add R4, R6, #200
		Load R2, NUM1
		Add R4, R2, R3
			(8)

2)		Explain big endian and little endian assignments and show how the byte addresses are assigned across words for each, with a diagram.	(4)
	A)		
	B)	Given x=0101 (multiplicand) and y=1010 (multiplier) in twos complement notation, compute the product using Booth's algorithm. Clearly show all the steps.	(8)
	C)	Write the block diagram and flowchart for unsigned binary multiplication.	(8)
3)		Divide 21 by 5 using restoring division technique. Clearly indicate all the steps.	(8)
	A)		
	B)	Represent the numbers 3.75 and 4.25 in IEEE 32 bit	(10)

		floating point format, perform the addition of the numbers in floating point representation using the rules for addition of floating point numbers and give the result in IEEE 32 bit floating point format.	
	C)	What are user visible registers? Give any one example.	(2)
4)		With a neat diagram, explain the Data Flow in the Fetch cycle of the processor.	(6)
	A)		
	B)	Give the sequence of microinstructions for the interrupt cycle and indirect cycle of the processor.	(6)
	C)	Draw the block diagram of a micro programmed Control Unit, explain the various components and the functioning of a micro programmed Control Unit.	(8)
5)		Describe any two disadvantages of Hardwired Control	(2)
	A)		
	B)	With a neat diagram, explain the operation of a single transistor dynamic memory cell. Also explain how the contents of the cell get refreshed during the read operation.	(6)
	C)	Explain the structure and operation of the read write head in a magnetic disk.	(6)
	D)	A computer has a small data cache capable of holding four words. Each cache block consists of one word. When a given program is executed, the processor reads data sequentially from the following addresses: 200, 201, 208, 213, 200, 216, 200, 201, 215, 201, 200,218, 220,200,201 (a) Assume that the cache is initially empty. Show the contents of the cache for an associative-mapped cache that uses the LRU replacement algorithm and compute the hit rate. (b) Repeat part (a) for an associative-mapped cache that uses the FIFO replacement algorithm and compute the hit rate.	(6)
6)		A block-set-associative cache consists of a total of 64 blocks, divided into 4-block sets. The main memory contains 4096 blocks, each consisting of 128 words. Assuming a 32-bit addressable address space, how many bits are there in each of the Tag, Set, and Word fields? Also calculate the number of bits in each of the fields of Direct and Associative mapping.	(4)
	A)		
	B)	Draw the structure of a 1M X 32 word addressable memory	(8)

using 256KX8 memory chips. Indicate clearly, the number of address lines and the data lines in the diagram.

C) With a neat timing diagram, explain the input transfer using multiple cycles, on synchronous bus. (8)

7) What is an interrupt? What is enabling and disabling of interrupts? Explain the sequence of events involved in handling an interrupt request from a single device. (8)

A)

B) With a neat block diagram, explain the operation of a parallel input interface. (8)

C) Explain coarse grained multithreading and fine grained multithreading. (4)

8) Explain the following with an example for each, with reference to pipelining (10)

A)

i) Data hazard
ii) Operand Forwarding
iii) Handling data dependencies in software

B) B. What is cache coherence problem in a shared multiprocessor system? Explain how this is addressed in the following approaches. (10)

(i) Write-through protocol
(ii) Write-back protocol

-----End-----