Question Paper

Exam Date & Time: 05-Jun-2018 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES
II SEMESTER B.Sc.(Applied Sciences) DEGREE MAKE UP- EXAMINATION - MAY / JUNE 2018
DATE: 5 JUNE 2018
TIME : 9.30 AM TO 12.30 PM

Computer Organization and Architecture [ICS 122]

Marks: 100 **Duration: 180 mins.**

Answer 5 out of 8 questions.

Missing data, if any, may be suitably assumed

1)		Discuss memory management requirements in detail.	(6)
	A)		
	B)	With a neat sketch explain address translation in virtual memory using translation lookaside buffer.	(8)
	C)	Explain the various functional units of a computer with a neat block diagram.	(6)
2)		What is interrupt latency? Explain the sequence of events involved in handling an interrupt request from a single device.	(4)
	A)		
	B)	Divide 5 by 2 using restoring division technique. Clearly show all the steps.	(6)
	C)	What is a hazard? When do data dependencies occur and how are they handled? Explain with suitable examples.	(10)
3)		Represent the following numbers 7.75 and 3.5 in IEEE 32-bit floating point format, perform 7.75 - 3.5 and give the result in IEEE 32-bit floating point format.	(6)
	A)		
	B)	Write the Block Diagram of Hardware for Addition and Subtraction and explain the same.	(6)
	C)	What is Direct Memory access? Explain the operation of DMA controllers in a computer system and also explain its connection to the processor with the help of a diagram	(8)
4)		Write a short note on Graphics processing unit.	(5)
	A)		
	B)		(10)

		Multiply -14 (Multiplicand) * 14 (Multiplier) using Booths algorithm. Clearly show all the steps.	
	C)	Draw a neat timing diagram of the input transfer using a single clock cycle on a synchronous bus and explain the same.	(5)
5)		Explain any 5 addressing modes with examples.	(10)
	A)		
	B)	Write a short note on the following i) Flash memory ii) EEPROM5C.	(4)
	C)	Explain how cache coherence problem is addressed in the following approaches in a shared memory multiprocessor system. i) Write through protocol ii) Write back protocol	(6)
6)		Discuss the following about magnetic hard disks with neat diagram(s): i) Mechanical structure ii) Read/Write head iii) Phase Encoding	(8)
	A)		
	B)	Give the sequence of microinstructions for the fetch cycle of the processor and explain the same	(6)
	C)	Explain the following with neat sketches i) Horizontal micro instruction ii) Vertical micro instruction	(6)
7)		Define the term 'Port'. Differentiate between serial and parallel port? With a neat sketch, explain Keyboard to processor connection using parallel port.	(8)
	A)		
	B)	Write a short note on Memory Hierarchy with a neat sketch.	(6)
	C)	Subtract the following using 2's complement arithmetic. Assume that the numbers are 4-bit numbers. State whether or not overflow occurs in each case? i) -7 from -3 ii) 1 from -7	(6)
8)		Draw and explain the Wilke's micro-programmed control unit.	(8)
	A)		
	B)	Give the value of the following 4-bit binary representation in sign and magnitude,1's complement and 2's	(6)

complement representations.

i) 1000

ii) 1111

C) With a neat sketch explain the functioning of the Microprogrammed Control Unit (6)

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