Question Paper

Exam Date & Time: 27-Apr-2018 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES
SECOND SEMESTER B.Sc (APPLIED SCIENCES)
END-SEMESTER THEORY EXAMINATIONS APRIL - 2018
DATE : 27 APRIL 2018
TIME : 9:30AM TO 12:30PM

Logic Design [IEC 121]

Marks: 100 **Duration: 180 mins.**

Answer 5 out of 8 questions.

Missing data, if any, may be suitably assumed.

1) A) A circuit has three inputs say, A, B and C. The output Z will be at logic '1' only if at least two or more inputs are at logic '1'. Simplify the function using K- map and implement using logic gates. (6)

B) Simplify the Switching function using K-Map. (8)

$F(A,B,C,D) = A'B'C'D' + A'B'C'D + A'BCD + AB'C'D + ABCD.$

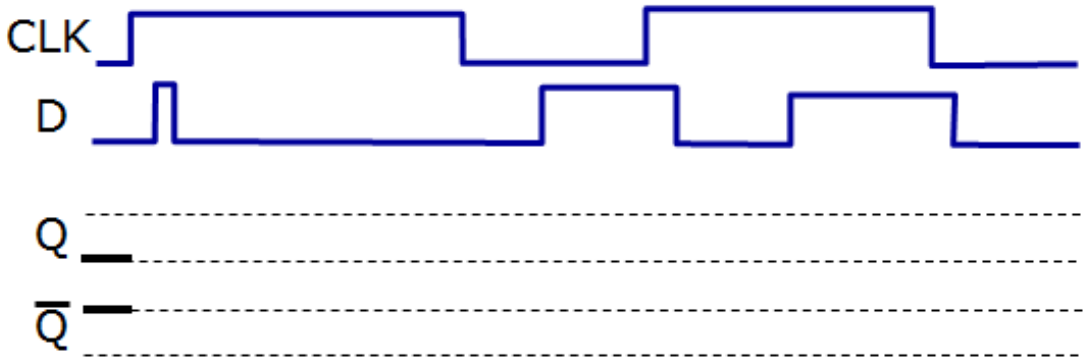
C) Draw the circuit diagram of S-R flip-flop using gates and write truth table. Show how JK flip flop can be converted to D flip flops. (6)

2) Simplify the Boolean function $F = \sum m(0,2,4,6) + d(5,7)$ (8)

A) and implement using logic gates.

B) Show that AB + AB'C+BC' = AC + BC'. (4)

C) Complete the timing diagram for D flip flop i) for negative edge triggered ii) for positive edge triggered iii) for level triggered. (8)



3) Minimize the following multiple output function using K-MAP (10)

A)

$$F1=\sum m(0,2,6,10,11,12,13)+d(3,4,5,14,15)$$

$$F2=\sum m(1,2,6,7,8,13,14,15)+d(3,5,12)$$

B) Implement a single digit BCD adder using 4bit Binary adder and additional gate (10)

4) Design a circuit for BCD to seven segment decoder (10)

A)

B) Design Half subtractor using only NAND gates (10)

5) Design a BCD to gray code converter using PLA . (10)

A)

B) Design a 2 bit UP-Down Asynchronous counter. (10)

6) Design 32:1 multiplexer using 4:1 mux. Write the truth table (10)

A)

B) Design 3:8 decoder using basic gates (10)

7) Design Full adder using only NAND Gates only (10)

A)

B) Design a 4bit Ring counter Explain with necessary timing waveform (10)

8) Solve the following: (10)

A)

a) Subtract 89.75 from 43.25 Using 2's compliment method

b) Add $(E0.5D)_{16}$ with $(49.F7)_{16}$

c) Add $(27.5)_8$ and $(74.4)_8$

B) Write the dataflow VHDL code for 3 input NAND and 3 input NOR gate (10)

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