Question Paper

Exam Date & Time: 04-May-2018 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES
THIRD SEMESTER B.S (ENGG)
END-SEMESTER THEORY EXAMINATIONS APRIL - 2018
DATE : 4 MAY 2018
TIME : 9:30AM TO 12:30PM

COMBINATIONAL AND SEQUENTIAL LOGIC [EC 231]

Marks: 100 **Duration: 180 mins.**

Answer 5 out of 8 questions.

1) A) (i) Add 548.6 + 280.37 in BCD number system (6)
(ii) Convert the following to the indicated bases (34F.B)16 = (?) $_8$ (84.3)10 = (?) $_2$
(iii) In an odd parity scheme which of the following contains an error
(a) 10110111_2 (b) 11101010_2

B) Design a combinational circuit to detect the decimal numbers 0,1,3,5 and 7 in a BCD input. (4)

C) Simplify the following function using karnaugh map and draw the circuit for the simplified expression using NAND gates. Also determine the essential prime implicant F(A,B,C,D)= $\sum$m(0,4,5,10,11,13,15) (5)

D) Write a dataflow VHDL code for 8 to 3 encoder (5)

2) A) Simplify the following Boolean expression (5)
(a) AB+(AC)'+AB'C(AB+C) (b)[A+(BC)']'(AB'+ABC)

B) Design a combinational circuit to convert BCD to gray code using basic gates. (5)

C) Using Quine Mccluskey method, Obtain the minimal sum for F(A,B,C,D)= $\sum$m(0,1,6,7,8,9,13,14,15) (10)

3) A) With a neat circuit diagram, explain the working of 4 bit binary adder/subtractor (5)

B) (5)

Implement the following function F(A,B,C,D) = $\sum$ m(0,1,3,4,8.9,15) using (i) 8:1 multiplexer and basic gates (ii) 4:1 multiplexer and basic gates

C) Implement the following multiple output combinational circuit using 4 to 16 decoder with active low outputs. (5)

$F1=\sum m(0,1,2,6)$ $F2=\sum m(2,4,6)$ $F3=\sum m(0,1,5,6)$ $F4=\sum m(0,1,4,7,12,14,15)$

D) Write a behavioral VHDL code for 8:1 multiplexer using case statement (5)

4) Implement the function $F=\sum m(0,2,4,6,7,8,10,12,13,15)$ (5)

A) using PLA.

B) Design a circuit for 4 to 2 priority encoder using basic gates (5)

C) Convert (i) JK flip-flop to SR flip-flop, (ii) SR flip-flop to T flip-flop (5)

D) Design a Mod 6 ripple up counter using T flip-flop (5)

5) Design a synchronous counter that goes through states 0,1,2,4,0,....The unused states must always go to zero (000) on the next clock pulse (10)

A)

B) Explain the operation of a master slave JK flip-flop with a neat circuit diagram (5)

C) Draw the logic diagram of gated SR latch using NAND gates. Derive the truth table for the same and explain its operation (5)

6) With a neat circuit diagram, explain the operation of 4 bit Universal Shift register for the following table (10)

A)

S_1	S_0	Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel load

B) Reduce the following state table and draw reduced state diagram (5)

Present State	Next State X=0	Next State X=1	Output X=0	Output X=1
A	B	C	1	0
B	F	D	0	0
C	D	E	1	1
D	F	E	0	1
E	A	D	0	0
F	B	C	1	0

C) Write the behavioral VHDL code for 4 bit parallel in serial out shift register (5)

7) Analyze the following synchronous sequential circuit. Draw the logic circuit, excitation table / state table and state diagram, X is the input, A&B are the outputs. (10)

A) $J_A=B$, $J_B=X'$, $K_A=X'B$, $K_B=A$ xor X

B) Design a Mealy type Sequence detector to detect an overlapping sequence "1010" (10)

8) Write the structural VHDL code for 8:1 multiplexer using 2:1 multiplexer (Code needs to be written for entire hierarchy). (10)

A)

B) Explain the operation of 4 bit Ring counter with a neat circuit diagram and suitable timing waveforms. (5)

C) Define the following terms with an example (5)
i) Self complementing code.
ii) Unit distance code.

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