Question Paper

Exam Date & Time: 02-Jun-2018 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES
IV SEMESTER B.S. DEGREE MAKE-UP EXAMINATION-MAY/JUNE 2018
DATE: 2 JUNE 2018
TIME: 9.30 AM TO 12.30 PM
Computer Architecture [CS 242]

Marks: 100 **Duration: 180 mins.**

Answer 5 out of 8 questions.

1)		Perform the following operations using 2's complement representation. Select enough bits to avoid overflow. (-2) - (-5) (-2) + (-7) (+3) + (+7) (-5) - (-7) (+6) - (-7)	(5)
	A)		
	B)	Draw the flowchart for floating point multiplication.	(5)
	C)	Draw the flowchart for integer division.	(5)
	i		
	ii	Divide 7 by 3 using integer division. Show all the steps.	(5)
2)		Discuss the evolution of PowerPC.	(5)
	A)		
	i		
	ii	With a suitable example, explain the use of stack in nested procedure calls.	(5)
	B)	Write the set of instructions using 0-address, 1-address, 2-address and 3-address instructions to evaluate the statement R=(A-B) / (C+D*E)	(10)
3)		Explain the Pentium and PowerPC addressing modes with neat diagrams.	(10)
	A)		
	B)	With neat drawings, discuss the instruction cycle with interrupt and indirect cycles.	(6)
	C)	Write the micro operations for ISZ (Increment and Skip if Zero) and BSA (Branch and Save Address) instructions.	(4)
4)		Discuss the different types of access methods in computer memory.	(8)
	A)		
	i		
	ii		(2)

Define access time and memory cycle time.

B) Discuss the functioning of micro-programmed control unit with a neat sketch. (10)

5) A computer system needs 512*8 RAM and 512*8 ROM. Design this memory system using 128*8 RAM and 512*8 ROM chips. Assume appropriate input and output signals for RAM and ROM chips. (10)

A)

B) i Describe magnetic disks. Explain the read and write mechanisms in magnetic disks with the help of a neat diagram. (7)

ii Distinguish between unified and split cache. (3)

6) A 4-way set-associative cache consists of a total of 64 lines (blocks). The main memory has 4096 lines, each consisting of 128 words. (8)

A)

- How many bits are there in a main memory address?
- How many bits are there in each of the TAG, SET and WORD fields?
- If the cache is an associative cache, how many bits will be there in each of the TAG and WORD fields?
- If the cache is a direct mapped cache, how many bits will be there in each of the TAG, LINE (BLOCK) and WORD fields? (4*2)

B) Discuss the concept of overlapped register windows. (12)

7) Explain the handshaking method of asynchronous data transfer. (10)

A)

B) Discuss pipeline processing with an example. (10)

8) Explain cache coherence problem with an example. Give two possible solutions for the same. (10)

A)

B) Write short notes on the following: (10)
i) Time shared common bus
ii) Interprocessor serial arbitration
iii) SIMD
iv) MIMD

-----End-----