Question Paper

Exam Date & Time: 20-Apr-2018 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES
FOURTH SEMESTER B.S. (ENGG)
END-SEMESTER THEORY EXAMINATIONS APRIL - 2018
DATE: 20 APRIL 2018
TIME: 9:30AM TO 12:30PM

Computer Architecture [CS 242]

Marks: 100 **Duration: 180 mins.**

Answer 5 out of 8 questions.

1. Answer ANY FIVE full Questions.
2. Missing data, if any, may be suitably assumed

1)	A)	Explain Booths algorithm for 2's complement multiplication with a neat flow chart. Multiply 7 and -6 using this algorithm.	(10)
	B)	Discuss DMA controller with a neat block diagram.	(10)
2)	A)	Draw a neat state diagram of the instruction cycle without interrupts and explain each state.	(10)
	B)	What do you mean by short IO and long IO wait? With necessary diagrams, write in detail the short I/O and long I/O waits with and without interrupts.	(10)
3)	A)	Write about register direct, memory direct, memory indirect, displacement and register indirect addressing modes. Draw diagram for each.	(10)
	B)	i) Discuss the register organizations of MC68000, 8086 and 80386. ii) Write the functions of instruction register, program counter and memory address register. (7+3=10MARKS)	(10)
4)	A)	With a neat diagram, write a short note on Multi-Port Memory.	(5)
	B)	For the following algorithm, design the control unit using hardwired implementation	(10)

```
begin
    m:=14;
    q:=5;
    i:=1;
    s:=0;
    while i <= m do
    begin
        j:= 1;
        while j<=q do
        begin
            s:=s+1;
            j:=j+1;
        end
        i:=i+1;
    end

end
```

C) Draw and explain Wilke's control (5)

5) With neat diagram discuss RAID 0, RAID 1, RAID 2, RAID 3 and RAID 4 levels. (10)

A)

B) i) Write about seek time and rotational latency, disk access time. (7)

ii) In a disk system there are 39 recording surfaces. The diameter of each recording surface is 50 cm and the inter-track gap is 0.5 mm. All the disks are double-sided disks except for one disk. There is an average of 360 sectors per track and each sector contains 512 bytes of data.

a) How many disk platters are there in the disk system?

b) What would be the maximum number of tracks in a double-sided disk?

c) How many cylinders shall be there in the entire system?

d) What would be the capacity of the disk system?

(3+4=7MARKS)

C) Define cache memory. Draw the diagram for a typical cache organization. (3)

6) Discuss the direct mapping technique with a neat Direct-Mapping Cache organization. (10)

A)

B) Compare RISC and CISC characteristics. (6)

C) Write a short note on memory management hardware. (4)

7) Explain the strobe control method of asynchronous data transfer with neat diagrams. (10)

A)

B) (10)

(i) Explain 32-bit IEEE floating point format.
(ii) (a) Represent 2.6875 in 32-bit floating point format.
(b) Interpret 10111101100000000000000000000000 using 32-bit floating point format.

(6+4=10MARKS)

8) Explain Flynn's taxonomy of parallel processor system with neat diagrams (10)

A)

B) ifferentiate between hardwired and micro-programmed control unit. (5)

C) Explain delayed branch of RISC pipeline with suitable examples (5)

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