Question Paper

Exam Date & Time: 01-Jun-2018 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES
IV SEMESTER B.S. DEGREE MAKE-UP EXAMINATION-MAY/JUNE 2018
DATE: 1 JUNE 2018
TIME: 9.30 AM TO 12.30 PM
VLSI Design [EC 245A]

Marks: 100 **Duration: 180 mins.**

Answer ANY FIVE full Questions.
Layout must be drawn using the graph sheet provided.
Missing data, if any, may be suitably assumed.

1) A) Derive the relationship between drain to source current Ids and voltage V_{ds} in resistive and saturation region for an enhancement type NMOS. (10)

B) The NMOS transistors in the circuit of Figure 1B have V_t= 1V, $\mu_n Cox$ = 120 $\mu A/V^2$ and L1=L2=L3= 1 μm. Find the required values of gate width for each of Q1,Q2 and Q3 to obtain the voltage and current values indicated. (10)

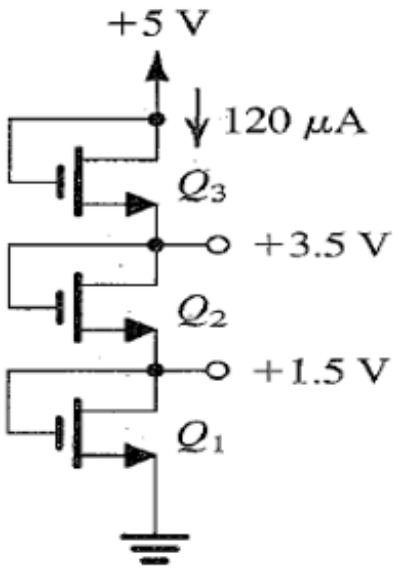

Figure 1B

2) Define latch-up in CMOS. Why does it occur? What are the (10)

A) remedies for latch- up? Explain in detail with necessary circuit diagrams and curve.

B) In CMOS inverter, if V_{DD} = 1.5V, V_{tn} = 0.4V, V_{tp} = -0.4V , Kn = 200 μA/V^2 and Kp = 100 μA/V^2: (10)

i) The peak current of 35μA occurs at 0.6V. What is (W/L)$_n$?

ii) What is the (W/L)$_p$?

3) A) With precise figures explain the different steps involved in the fabrication of NMOS transistor. What is the advantage of the self-aligned process? (10)

B) Draw the circuit, stick diagram and layout of two input NAND gate using NMOS design style. (10)

4) A) Explain the working and draw transfer characteristic of NMOS inverter with (10)

i) Resistor pull-up

ii) Depletion mode transistor pull-up

iii) Enhancement mode pull-up

B) Discuss the operation of 6T SRAM in detail. (10)

5) A) Explain different scaling models. Discuss the effect of different scaling on following parameters: (10)

[i] Gate oxide capacitance C_g [ii] Channel resistance R_{on} [iii] Gate delay T_d

B) Implement Boolean function F = (x + y)[z + (w.t)(z+ x)] using (10)

i) CMOS logic

ii) NMOS logic

iii) pseudo NMOS logic.

6) Given that 1$\square$Cg = 0.01 pF. (10)

A) Find the optimal number of NMOS inverters to be cascaded so as to drive an off-chip capacitive load of 0.54 pF such that the total delay is minimized.

Give the cascaded structure, clearly showing the L:W ratio.

Show the delay T_d across each inverter stage and hence calculate the overall delay.

B) An enhancement type NMOS has V_t= 0.8V and μ_nCox = 20 μA/V^2 (10)

i)Find (W/L) for V_G=2.8V, V_D=5V, V_S=1V and I_D=0.24mA.

ii) Calculate ID for V_G=5V, V_D=4V, V_S=2V for same (W/L) as in part (i)

7) A) What is a cross-bar switch? Bring out the differences between barrel shifter and cross-bar switch.Give the circuit implementation and the stick notation of 4X4 barrel shifter. (10)

B) Give hardware implementation and draw stick diagram for storing following 4-bit words using NMOS ROM structure. word1: 0101; word2: 0010 ; word3: 1001 ; word4: 0110 (10)

8) A) Calculate the effective capacitance for the given multi-layer structure in Figure 8A for 5μm process. Relative Capacitance value for metal1= 0.075, polysilicon=0.1 and Gate-to-channel = 1.0. (10)

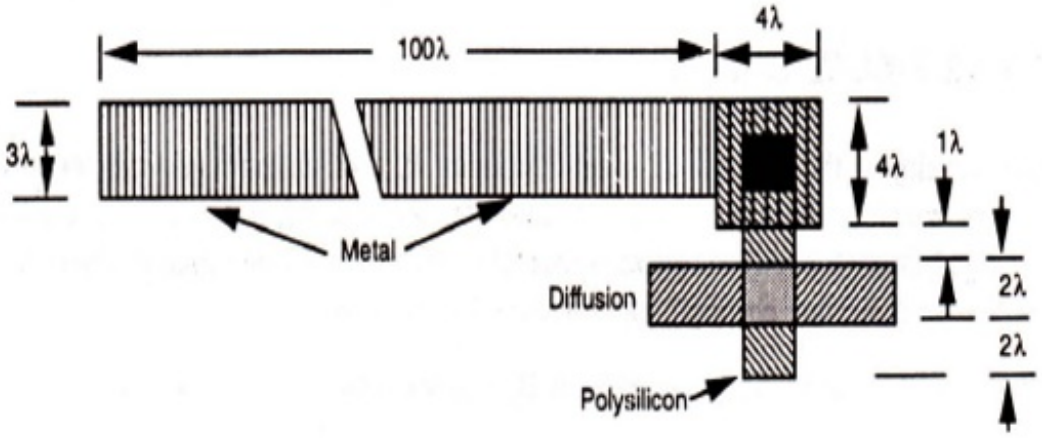

Figure 8A

B) Discuss cascaded inverters as drivers for driving large capacitive loads and derive the necessary expressions. (10)

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