Question Paper

Exam Date & Time: 18-Apr-2018 (09:30 AM - 12:30 PM)

MANIPAL ACADEMY OF HIGHER EDUCATION

INTERNATIONAL CENTRE FOR APPLIED SCIENCES
FOURTH SEMESTER B.S (ENGG)
END-SEMESTER THEORY EXAMINATIONS APRIL - 2018
DATE : 18 APRIL 2018
TIME : 9:30AM TO 12:30PM
VLSI Design [EC 245A]

Marks: 100 **Duration: 180 mins.**

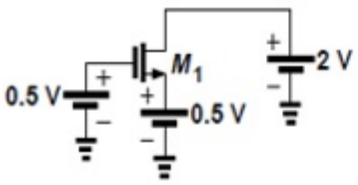
Answer 5 out of 8 questions.

Layout must be drawn using the graph sheet provided.
Missing data, if any, may be suitably assumed.

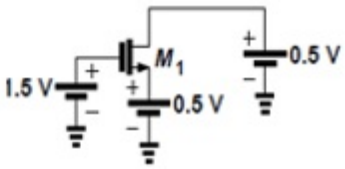
1) Explain the working of an enhancement type NMOS transistor in cut- off, linear and saturation region. Plot the current-voltage characteristics. (10)

A)

B) Find the region of operation for NMOS based circuits given in **Figure 1B**. Assume $V_T = 0.4V$. (10)



(i)



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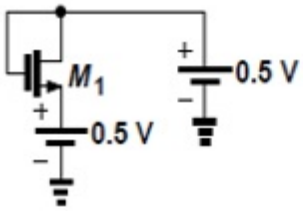
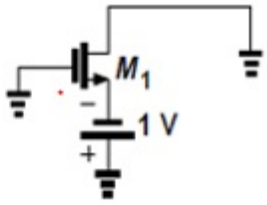


(iii)



(iv)

Figure 1B

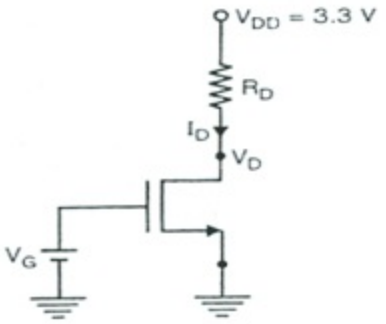
2) Discuss the second order effects of MOSFET in detail with necessary diagrams and equations. (10)

A)

B) (10)

The MOSFET in **Figure 2B** has V_t= 1V and $\mu_n Cox$ = 1 mA/V^2 . Find the drain current and drain voltage for V_G = 2V and R_D = 10kΩ.

Figure 2B



3) A) With precise figures explain the different steps involved in the fabrication of CMOS using SOI technique. (10)

B) Draw the circuit, stick diagram and compact layout for p-well CMOS inverter for $\beta_n = \beta_p$ (10)

4) A) Explain the operation of pseudo NMOS inverter. Derive Z_{pu}/Z_{pd} ratio for pseudo NMOS inverter driven from a similar inverter. (10)

B) Give the circuit implementation of following multiple output functions using NMOS based PLA. Give the stick notation. (10)

$$Z_1 = AB + \bar{A}\bar{B}C\ ;\ Z_2 = AB\ ;\ Z_3 = A + \bar{B}C.$$

5) A) State and explain the three different scaling models. Discuss the effect of scaling using Combined V and D, Constant E and Constant V models on following parameters: [i] Gate area A_g [ii] Gate capacitance per unit area C_o [iii] Carrier density in channel Q_{on} [iv] Maximum operating frequency f_o . (10)

B) Derive the expression for rise time estimation and fall time estimation of CMOS inverter. What are the significance of rise time and fall time? (10)

6) A) Calculate the effective input capacitance for the given multi-layer structure in **Figure 6A** for 5μm process. Relative Capacitance value for metal1= 0.075, polysilicon=0.1 and Gate to channel = 1.0. (10)

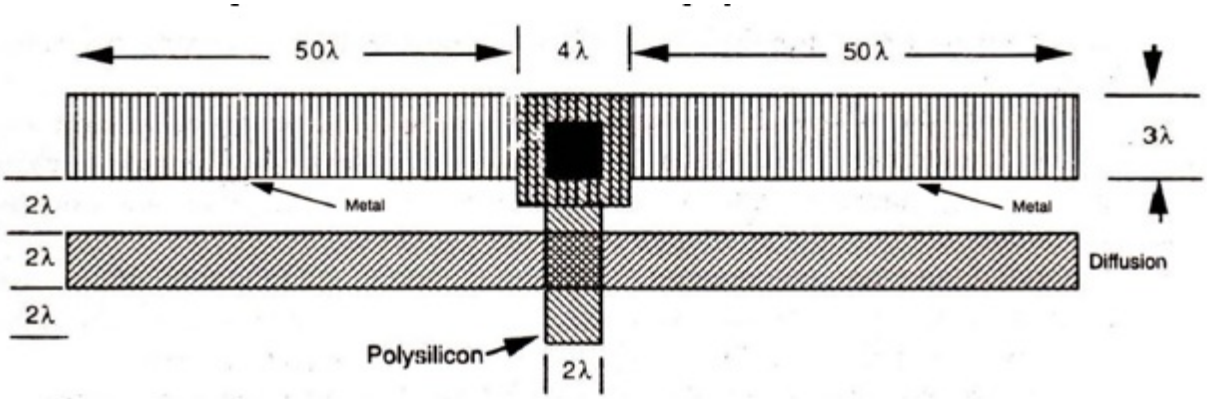


Figure 6A

B) Write ten differences between CMOS technology and Bipolar Technology. (10)

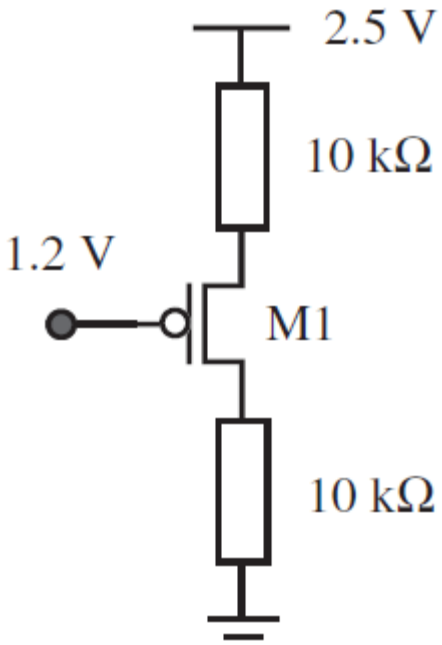
7) Explain structured implementation of N-bit bus arbitration logic. Give the stick notation. Discuss the suitability of implementation using NMOS/ CMOS technology (10)

A)

B) Implement the following 2 input logic function using Transmission gate approach (10)
[i] AND gate [ii] OR gate [iii] NAND gate [iv] NOR gate

8) Calculate I_D and V_{SD}, and indicate the region of operation of transistor M_1 for the circuit in Figure 8A. V_{tp} = -0.4 V, K_p = $120\mu A/V^2$, and W/L = 2. (10)

A)



B) Two CMOS inverters are cascaded to drive a capacitive load $C_L = 40\square C_g$ as shown in **Figure 8B**. Find the Z_{pu} and Z_{pd} of each inverter. Calculate the pair delays in terms of τ for the inverter geometry indicated in figure for rising step input and falling step input. (10)

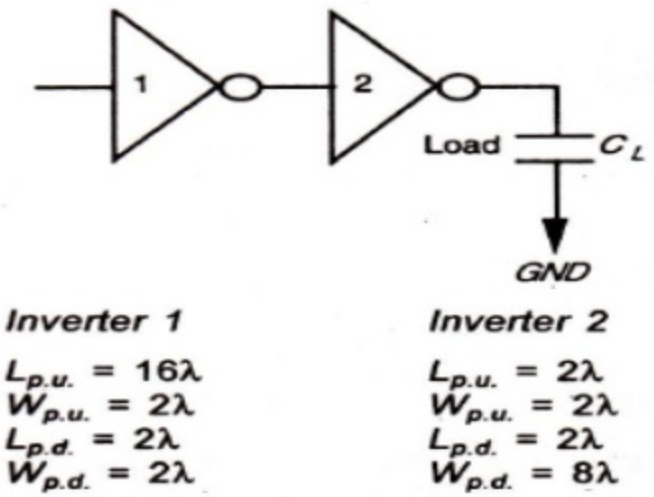


Figure 8B

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