Reg. No.										

MANIPAL INSTITUTE OF TECHNOLOGY

MANIPAL

(A constituent unit of MAHE, Manipal)

SECOND SEMESTER B.Tech. DEGREE END SEMESTER EXAMINATION
APRIL/MAY 2018
SUBJECT: BASIC ELECTRONICS (ECE - 1001)

TIME: 3 HOURS **MAX. MARKS: 50**

Instructions to candidates
- Answer **ALL** questions.
- Missing data may be suitably assumed.

1A. Highlight the main drawback of fixed bias circuit for BJT. How it is overcome in self- bias circuit? Determine I_B, I_C, V_{CE}, V_B and V_E for the voltage divider configuration shown in figure Q1A. (Given: V_{CC}=12V, R_1=39kΩ, R_2=8.2kΩ, R_C= 3.3kΩ, R_E=1kΩ). Silicon BJT with β=120 is used.

1B. Draw the equivalent circuits and characteristic curves for forward bias of i) Ideal diode ii) Diode with specific cut-in voltage and forward resistance. Mention approximate values of cut-in voltage for Silicon and Germanium diodes.

1C. Draw the circuit of Non inverting Amplifier using OPAMP. Write the expression for voltage gain for this amplifier.

(5+3+2)

2A. Draw the circuit of Zener Regulator. Explain line & Load regulation and how this is achieved in it. For a Zener Regulator V_i= 16 V, series resistance R_S= 1 K, V_Z= 10 V and R_L= 3 K. Determine V_o, I_Z and P_Z.

2B. Implement NOT, AND and OR logics using only NAND gates.

2C. Explain the working of 2-input OR gate using discrete components.

(5+3+2)

3A. Simplify the following expression:

i) $Y = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}\bar{C} + A\bar{B}C + AB\bar{C} + ABC$ Using K-maps

ii) $Y = \bar{A}(A + B) + (B + AA) + (A + \bar{B})$ Using Boolean algebra

3B. With the help of logic diagram and timing diagram, explain the working of 3 bit negative edge triggered asynchronous up counter.

3C. The data 10101 is given to the input of a 5 bit shift register. How many clock cycles are required to: i) Get the MSB at the output if it is a Serial in serial out shift register?
ii) Load the data into the register.

(5+3+2)

4A. Draw the logic circuit and write the truth table of (i) SR Flip flop. (ii) J-K Flip flop (ii) T Flip flop.

4B. For data bit stream of 1 0 1 1 0, draw the waveforms if the modulation performed is i) ASK ii)

PSK and iii) FSK.

4C. State Nyquist sampling theorem. Specify the sampling frequency to sample message signal that ranges between 300 Hz to 3.4 KHz.

(5+3+2)

5A. Calculate carrier frequency, carrier amplitude, modulating frequency, frequency deviation and bandwidth for a FM modulated signal given by the equation

$$V_{FM}(t) = 5\cos\left(2x10^{8}\pi t + 3\sin(40000\,\pi t)\right)$$

5B. List and briefly explain multiple access technologies.

5C. Certain AM transmitter radiates 10 kW of power with carrier unmodulated and 11 kW of power when carrier is sinusoidally modulated. Calculate the modulation index.

(5+3+2)

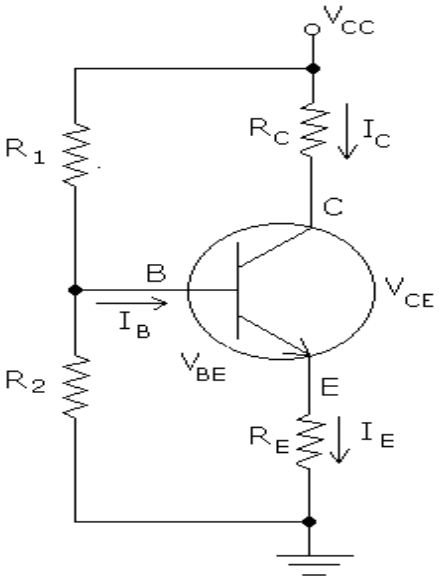

Figure Q1A